

Exhibit B

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ZTE Corporation, ZTE (USA), Inc., and ZTE (TX), Inc.,

Petitioner,

v.

WSOU Investments LLC D/B/A Brazos Licensing and Development,

Patent Owner.

U.S. Patent No. 8,179,960

Case No. IPR2021-00696

PETITION FOR *INTER PARTES* REVIEW

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LIST OF EXHIBITS

Exhibit	Description
Ex-1001	U.S. Patent No. 8,179,960 (the '960 patent)
Ex-1002	Prosecution File History of U.S. Patent No. 8,179,960
Ex-1003	Declaration of Tal Lavian, Ph.D.
Ex-1004	Curriculum Vitae of Tal Lavian, Ph.D.
Ex-1005	U.S. Patent Application Publication No. 2006/0146934 to Caglar (" <i>Caglar</i> ")
Ex-1006	U.S. Patent Application Publication No. 2005/0286634 to Duvivier (" <i>Duvivier</i> ")
Ex-1007	Video coding with H.264/AVC: Tools, Performance, and Complexity by Ostermann et al. (2004)
Ex-1008	Overview of the H.264/AVC Video Coding Standard by Wiegand et al. (July 2003) (" <i>Wiegand</i> ")
Ex-1009	U.S. Patent Application Publication No. 2008/0151999 to Youn et al. (" <i>Youn</i> ")
Ex-1010	The H.264/MPEG4 Advanced Video Coding Standard and its Applications by Marpe et al. (Aug. 2006)
Ex-1011	The H.264/AVC Video Coding Standard by Weigand et al. (Mar. 2007)
Ex-1012	Excerpts of IEEE-Wiley Dictionary (2004)
Ex-1013	International Publication No. WO 2008/008331 A2 to Su et al.
Ex-1014	Variable Block Size Motion Estimation Hardware for Video Encoders, Chinese Univ. of Hong Kong, by Li (Nov. 2006)
Ex-1015	MPEG-4 Part 10 AVC (H.264) Video Encoding, Scientific Atlanta (Jun. 2005)
Ex-1016	The H.264/AVC Advanced Video Coding Standard: Overview and Introduction to the Fidelity Range Extensions, Microsoft Corporation, by Sullivan et al. (Aug. 2004)
Ex-1017	The emerging H.264/AVC Standard, Heinrich Hertz Institute, by Schäfer et al. (Jan. 2003)
Ex-1018	A Study of MPEG-2 and H.264 Video Coding, Purdue Univ., by Igarta (Dec. 2004)
Ex-1019	RTP Payload Format for H.264 Video, The Internet Society, by Hannuksela et al. (Jun. 26, 2003)

I. PRELIMINARY STATEMENT

ZTE Corporation, ZTE (USA), Inc., and ZTE (TX), Inc., (collectively “ZTE”) requests *inter partes* review of claims 1-28 of U.S. Patent No. 8,179,960 (Ex-1001). WSOU Investments LLC (“WSOU”) asserts the ’960 patent against ZTE in WSOU Investments LLC v. ZTE Corporation et al., 6:20-cv-00490-ADA (W.D. Tex.) (“Litigation”).

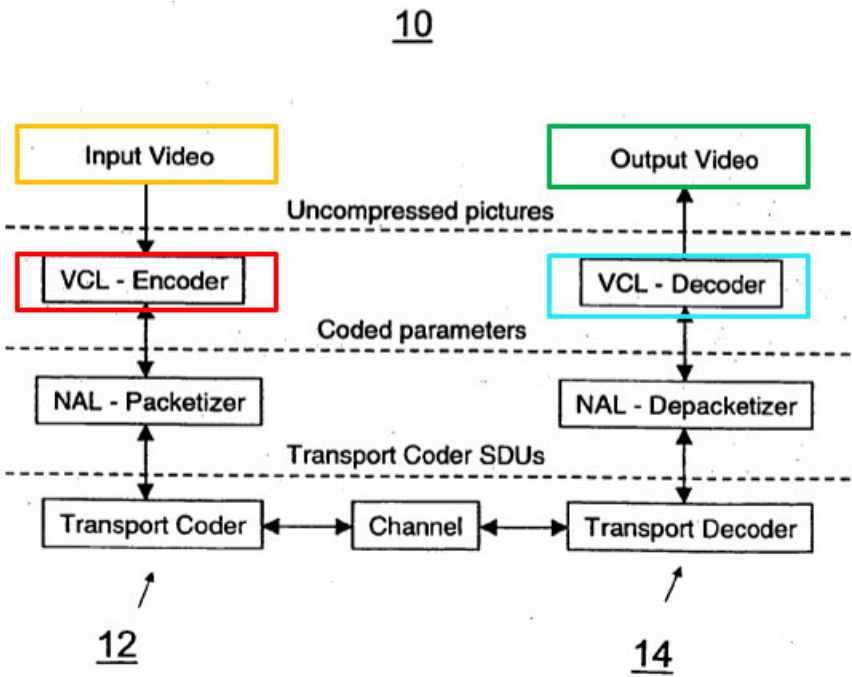
The ’960 patent describes coding and decoding methods and apparatuses, but the disclosed coding and decoding methods were already well known in the prior art.

No	Claim Limitation
1p	A method for generating an encoded video signal from an original video signal, the original video signal comprising a sequence of video frames , the encoded video signal for use in a subsequent video display of said original video signal , the method comprising the steps of:
1A	generating virtual reference data based on a portion of the original video signal , wherein the generated virtual reference data does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof ;
1B	encoding, using a processor, said generated virtual reference data and incorporating said encoded virtual reference data into the encoded video signal ;
1C	incorporating into the encoded video signal an indication that said encoded virtual reference data incorporated therein comprises data which does not represent any portion of any individual frame

	of the original video signal to be displayed in said subsequent video display thereof;
1D	encoding, using a processor, one or more portions of the original video signal which are to be displayed in said subsequent video display thereof, wherein said encoding of said one or more portions of said original video signal which are to be displayed are based on and specifically reference a portion of said encoded virtual reference data; and
1E	incorporating said encoded portions of said original video signal which are to be displayed into said encoded video signal.

Ex-1001, Claim 1 (Annotated).

Caglar (Ex-1005), *Duvivier* (Ex-1006), and *Youn* (Ex-1009) disclose encoding and decoding a video signal using a virtual frame like that claimed the '960 patent. Alone or when combined in routine, predictable ways, *Caglar*, *Duvivier*, and *Youn*—none considered by the USPTO for the '960 patent—anticipate and render obvious all features of the challenged claims.



Ex-1005, FIG. 16.

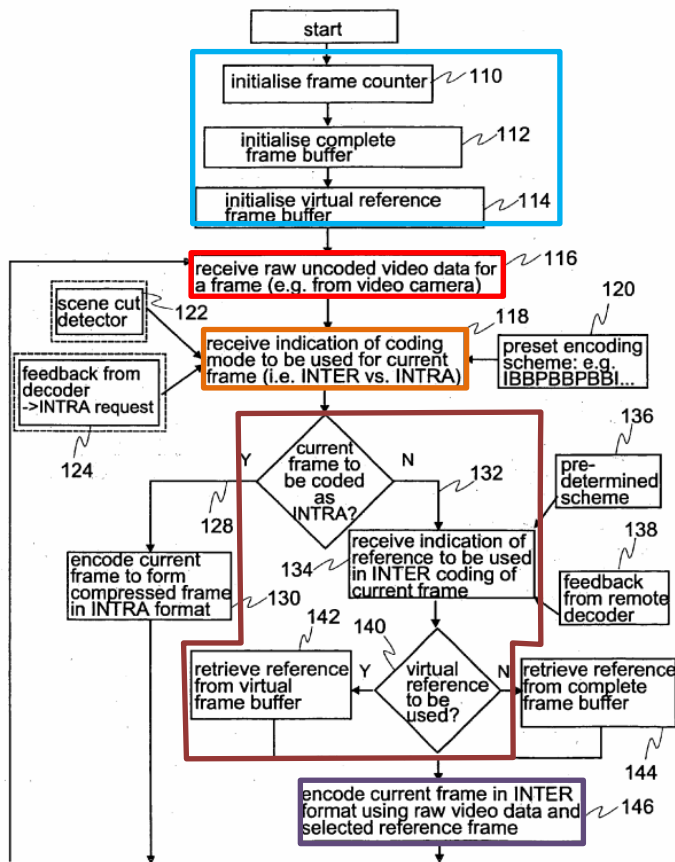


Fig. 18a

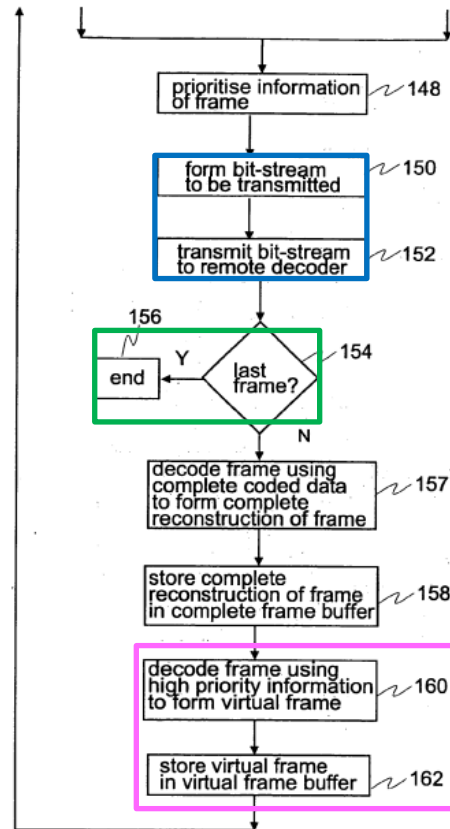


Fig. 18b

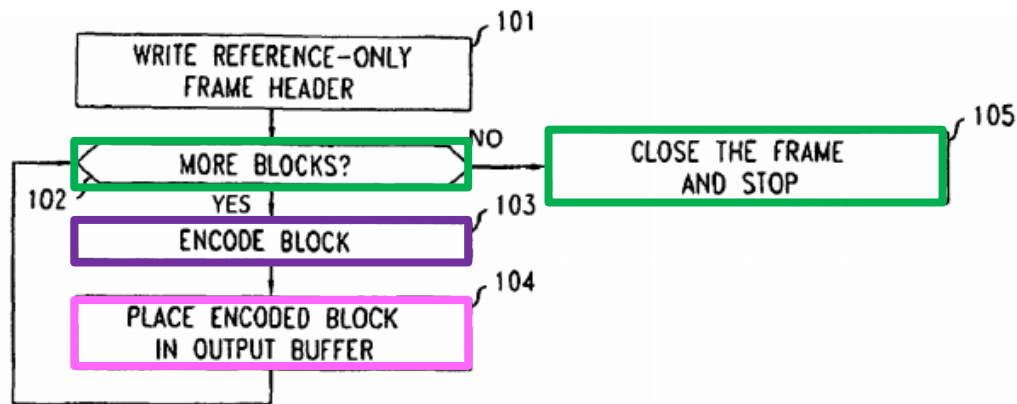
(Left) Ex-1005, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

II. OVERVIEW OF THE '960 PATENT

Like *Caglar*, *Duvivier*, and *Youn*, the '960 patent describes devices and methods for coding and decoding videos using reference frames under the well-known video coding standards authored by the International Telecommunication Union (ITU). Ex-1001, Abstract, 1:15-23, 5:14-18; Ex-1005, Abstract, ¶[0017]; Ex-1006, ¶¶[0003]-[0004], [0021]-[0022]; Ex-1008, 1; Ex-1009, ¶[0002].

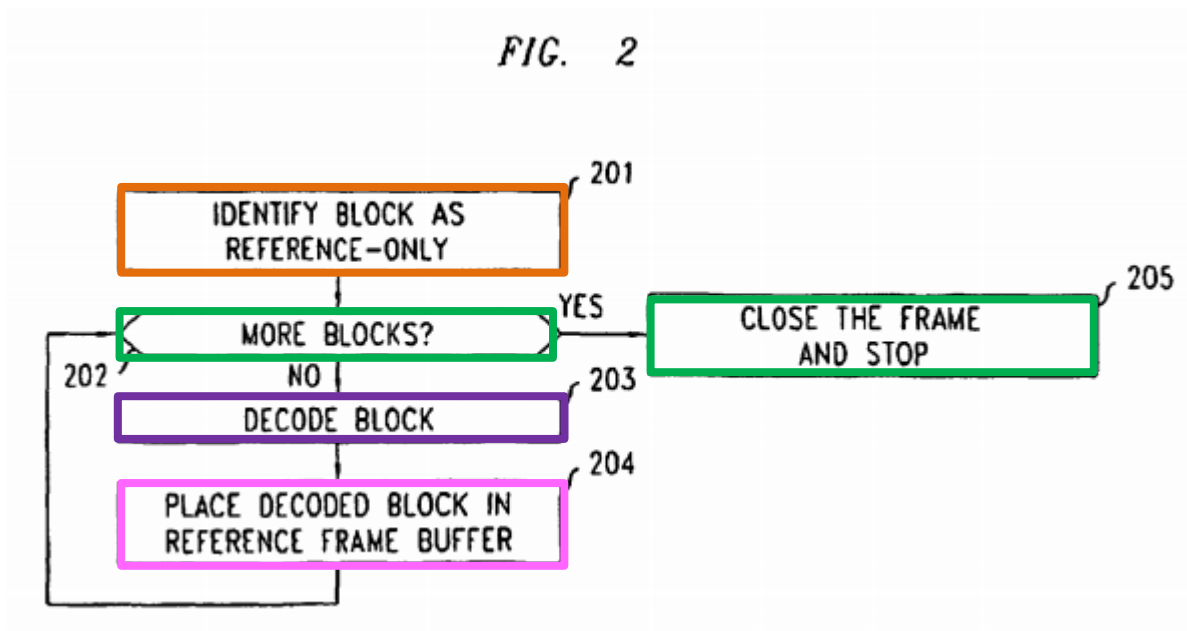
Fig. 1 shows an embodiment of a method of encoding a video signal with use of virtual reference data. Ex-1001, 3:11-13. A header is written into a frame or

slice in box 101, *id.*, 5:18-20, and then, box 102 decides whether “more video blocks in the virtual reference frame (or slice) to be encoded.” *Id.*, 5:18-20. If not, box 105 “closes the frame (or slice) and the flow terminates.” *Id.*, 5:23-24. If more video blocks are encoded, they are encoded in box 103. *Id.*, 5:20-23. In step 104, the encoded video block is placed “in an output buffer” for subsequent use. *Id.*; 5:20-27.



'960 Patent, Fig. 1 (annotated).

Fig. 2 shows an embodiment of a method of decoding a video signal with use of virtual reference data. *Id.*, 3:11-13. For box 201, the frame to be decoded is identified as “a virtual reference (only) frame (or slice).” *Id.*, 5:31-33. Then, box 202 “decides whether there are more video blocks to be decoded.” *Id.*, 5:33-34. If not, box 205 the “flow terminates.” *Id.*, 5:37-38. If there are more video blocks to be decoded, a next video block is decoded in box 203. *Id.*, 5:34-37. Then, in box 204, the decoded video block is placed in a buffer for subsequent use. *Id.*, 5:34-41.



Ex-1001, Annotated Fig. 2.

III. OVERVIEW OF PRIOR ART

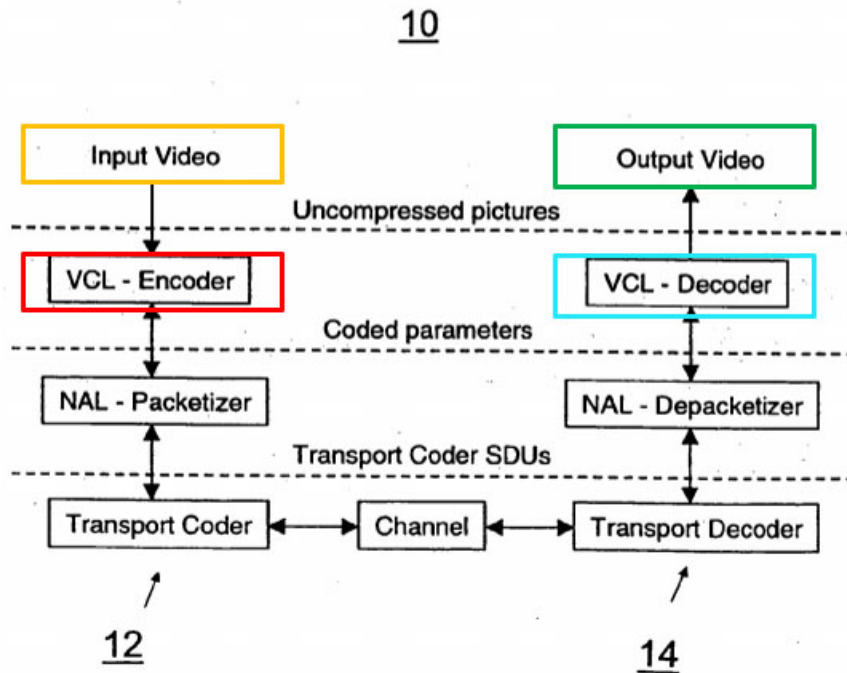
The '960 patent was filed on November 12, 2008, and does not claim priority to a prior application. November 12, 2008 is thus the '960 patent's earliest possible priority date.

Before the '960 patent, encoding and decoding video transmissions had been in use for years. *See* Ex-1005; Ex-1006; Ex-1007; Ex-1008; Ex-1010; Ex-1011, *see also* Ex-1003, ¶48.

A. *Caglar*

U.S. Patent Pub. No. 2006/0146934 (Ex-1005, “*Caglar*”) was published on July 6, 2006, and filed on March 6, 2006. *Caglar* is therefore prior art to the ’960 patent under 35 U.S.C. § 102(b).

Caglar describes methods for “encoding a video signal.” Ex-1005, Abstract, ¶¶[0103], [0111]. *Caglar* discloses in Figure 16 below that shows an uncompressed video signal is encoded and compressed to create an encoded video signal that is sent to a decoder to create an output video. *Id.*, ¶[0059].



Id., FIG. 16.

Caglar discloses FIGS. 18 and 19 that illustrate encoding and decoding procedures. *Id.*, ¶¶[0229], [0238]; *see also* ¶¶[0230], [0237]; FIGS. 18a, 18b, 19. In

FIG. 18, steps 110, 112, 114 initialize the procedure, *id.*, ¶[0238], step 116 includes receiving “raw uncoded video data for a frame” from a source or a live feed, *id.*, FIG. 18, ¶[0238], and step 118 determines if the frame is “to be an INTRA frame or an INTER frame.” *Id.*, ¶[0238]. INTRA frames are compressed images that are not predicted on other frames or at all and INTER frames are compressed images that are predicted on other frames. *Id.*, ¶¶[0013]-[0014]. For coding a frame as an INTER frame, determined in step 132, *Caglar* discloses receiving “an indication of a frame to be used as a reference in encoding the current frame in INTER frame format” in step 134. *Id.*, ¶[0240]. If so, in step 140 “the encoder determines whether a virtual reference is to be used.” *Id.* And then, in step 142, “[i]f a virtual reference frame is to be used, it is retrieved from the virtual reference frame buffer.” *Id.*, ¶[0241]. Once the virtual reference frame is selected, in step 146, the frame is encoded including the raw video data and the selected reference frame. *Id.*, FIG. 18a, ¶[0241].

Once the frame is encoded, the bit-stream is encoded and transmitted in steps 150 and 152. *Id.*, ¶[0241]. If the last frame, the process ends in steps 154 and 156. *Id.*, ¶[0240]. If the last frame, a virtual frame is created “on the basis of the relevant reference frame using only the high priority data in order to form a reconstruction of a virtual frame” and stored in the buffer in steps 160 and 162. *Id.*, ¶[0241]. This process is shown in FIG. 18 below.

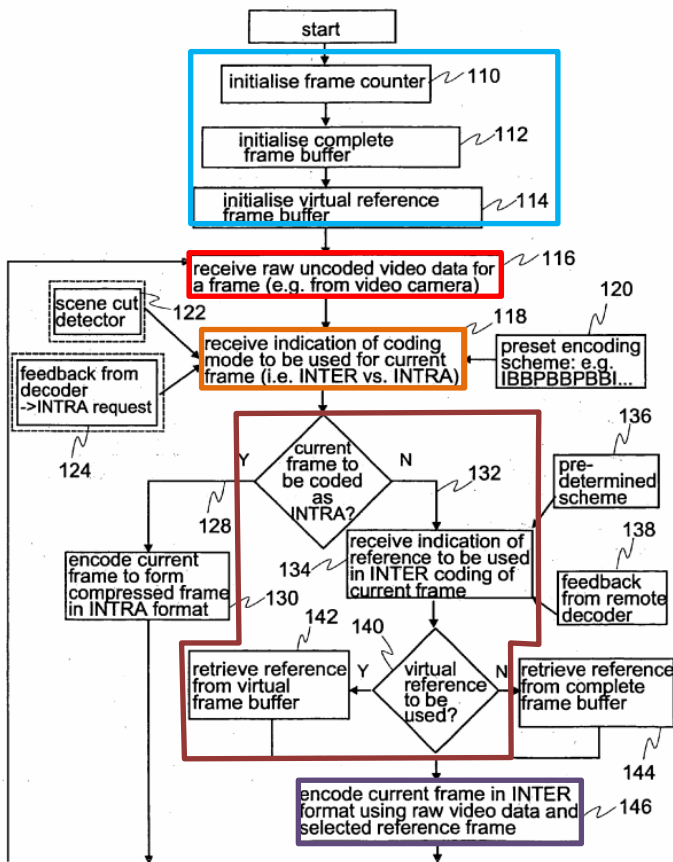


Fig. 18a

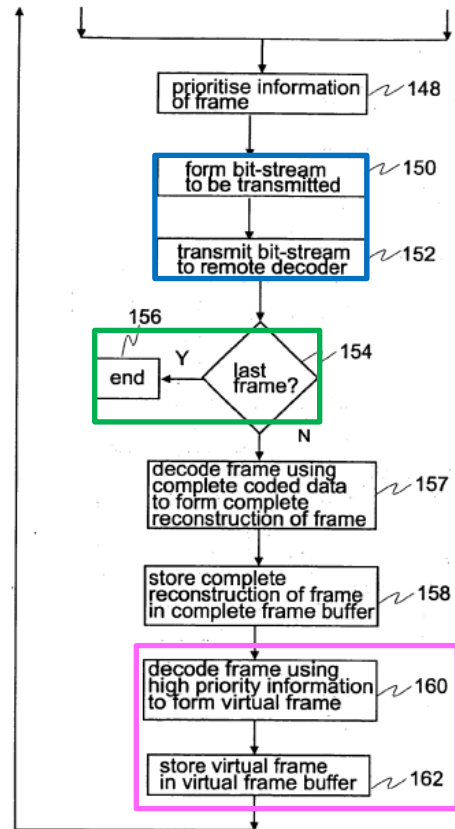


Fig. 18b

(Left) Ex-1005, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

Caglar discloses a corresponding decoding method in FIG. 19. *Id.*, FIG. 19.

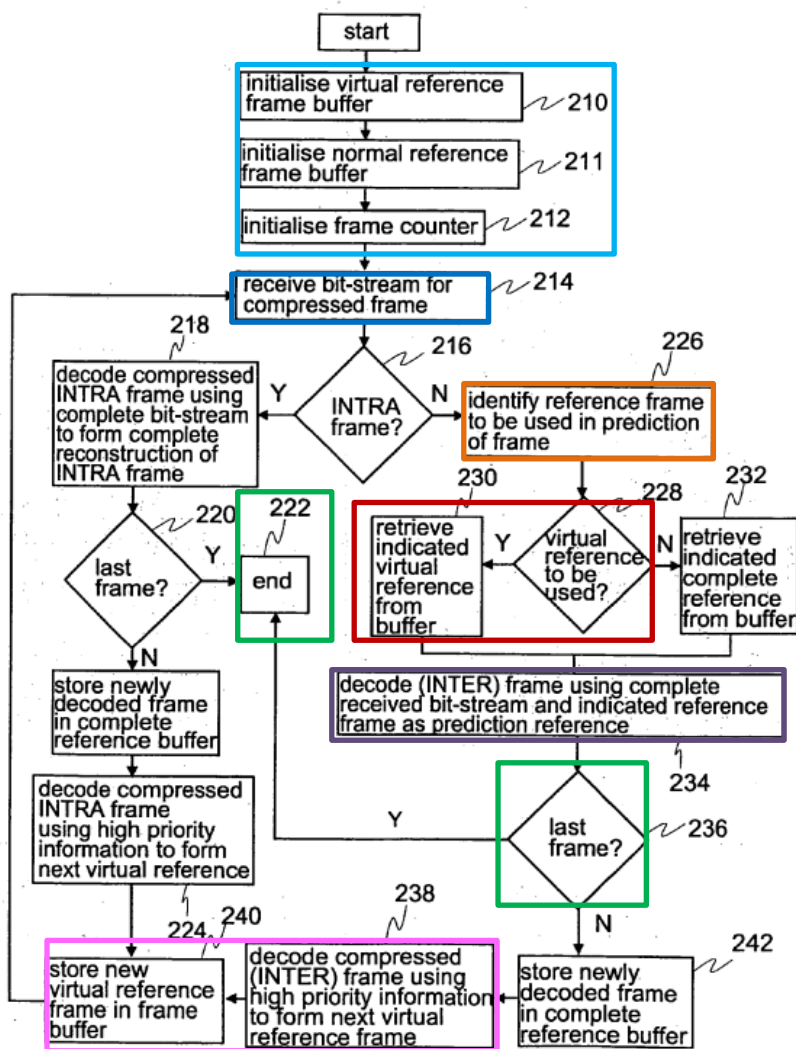


Fig. 19

Caglar, Annotated Fig. 19.

B. Duvivier

U.S. Patent Pub. No. 2005/0286634 (Ex-1006, “Duvivier”) was published on December 29, 2005 and filed on March 1, 2005, making it prior art under 35 U.S.C. § 102(b).

Duvivier describes methods for efficiently storing data for a slice of a video frame where each frame is comprised of multiple macroblocks. Ex-1006, Abstract, ¶[0004]. *Duvivier* discloses a method of forming a macroblock for “efficient processing of the partition data” and “encoding and decoding of video data streams.” *Id.*, ¶¶[0002], [0021].

C. *Youn*

U.S. Patent Pub. No. 2008/0151999 (Ex-1007, “*Youn*”) was published on June 26, 2008 and filed on Dec. 22, 2006, making it prior art under 35 U.S.C. § 102(b) or at least 35 U.S.C. § 102(e).

Youn discloses efficiencies to be had when comparing a macroblock from an input frame to a predicted macroblock. Ex-1009, ¶[0011]. Accordingly, *Youn* discloses “a method for bypassing transform and quantization steps in a video compression.” *Id.*, Abstract. *Youn* discloses that “[i]n In H.264, video data is compressed using a transform step, such as a discrete cosine transform (DCT), and a quantization (Q) step.” *Id.*, ¶[0002]. But, these computations are undesirable because they “are computationally intensive,” and thus it is advantageous to skip these computations if possible. *Id.* *Youn* discloses a method for bypassing these steps by determining whether transform coefficients may be quantized to zero based on a sum of absolute transformed differences (SATD) rather than using the conventional method of determining a sum of absolute difference (SAD). *Id.*,

¶¶[0002]-[0003]. *Youn* thus discloses a method of efficiently determining whether transform coefficients may be quantized to zero, and if not, the conventional method of quantizing transform coefficients is used. *Id.*, ¶¶[0026]-[0027].

IV. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art may be reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). A person of ordinary skill in the art (“POSA”) at the time of the purported invention would have had a Bachelor of Science degree in Electrical Engineering or an equivalent field, with at least two years of academic or industry experience in video data transmission or comparable industry experience. Ex-1003, ¶36. With more education, for example, postgraduate degrees and/or study, less experience is needed to attain an ordinary level of skill in the art. Similarly, more experience can substitute for formal education. Ex-1003, ¶36.

V. CLAIM CONSTRUCTION

Only claim terms “in controversy” need be construed in IPR “and only to the extent necessary to resolve the controversy.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citation omitted), *cert. denied*, 138 S. Ct. 1695 (2018).

In the District Court, Petitioner and Patent Owner have offered the following terms for construction, *see* Litigation, Dkt. 57, p. 9, after the number of terms have been narrowed:

Claim	Term	Petitioner's Proposed Construction	Patent Owner's Proposed Construction
1, 2, 3, 9, 10, 15, 16, 17, 23, and 24	"virtual reference"	A group of pixels used as reference material for encoding portions of the video signal, but that does not comprise or represent any portion of the actual video sequence to be displayed.	a group of pixels (e.g., a block) that is used as reference material for encoding portions of the video signal (e.g., a motion-compensated inter-predicted block), but that does not comprise or represent any portion of the actual video sequence to be displayed.
1, 9, 15, 23	"does not represent any portion of any individual frame of the original video signal"	Data generated based on a portion of a video signal but not to be displayed with the video signal.	Plain and Ordinary Meaning
3, 17	"minimize differences"	Indefinite	Plain and Ordinary Meaning

For the purpose of this *Inter Partes Review*, Petitioner adopts Patent Owner's constructions for the above terms. Moreover, given the similarities between the prior art and the disclosure of the '960 patent, no express construction of these

terms is needed, except the term “virtual reference data” as discussed below, to determine whether the claims are unpatentable.

A. “virtual reference data”

The '960 Patent states, “a ‘virtual reference,’ as used herein, is defined as Patent Owner’s Proposed Construction listed in the chart above. Ex-1001, Abstract, 2:17-22. Because the '960 patent provides an explicit definition for this term, the Board should adopt this definition for purposes of this *Inter Partes Review*.

VI. STATEMENT OF PRECISE RELIEF REQUESTED

1. Claims for Which Review Is Requested

Petitioners respectfully request review under 35 U.S.C. § 311 of claims 1-25 of the '960 patent and cancellation of those claims as unpatentable.

2. Statutory Grounds

This petition presents the following grounds of unpatentability:

Ground	References	Basis	Challenged Claim(s)
1	<i>Caglar</i> in view of <i>Duvivier</i>	§ 103	1, 2, 6-16, 20-28
2	<i>Caglar</i> in view of <i>Duvivier</i> and <i>Youn</i>	§ 103	3-5, 17-19

**VII. GROUND 1: CLAIMS 1, 2, 6-16, AND 20-28 UNPATENTABLE OVER
CAGLAR ALONE OR IN VIEW OF DUVIVIER**

A. Claim 1

Caglar renders obvious claim 1 alone and/or in combination with *Duvivier*.

Ex-1003, ¶64.

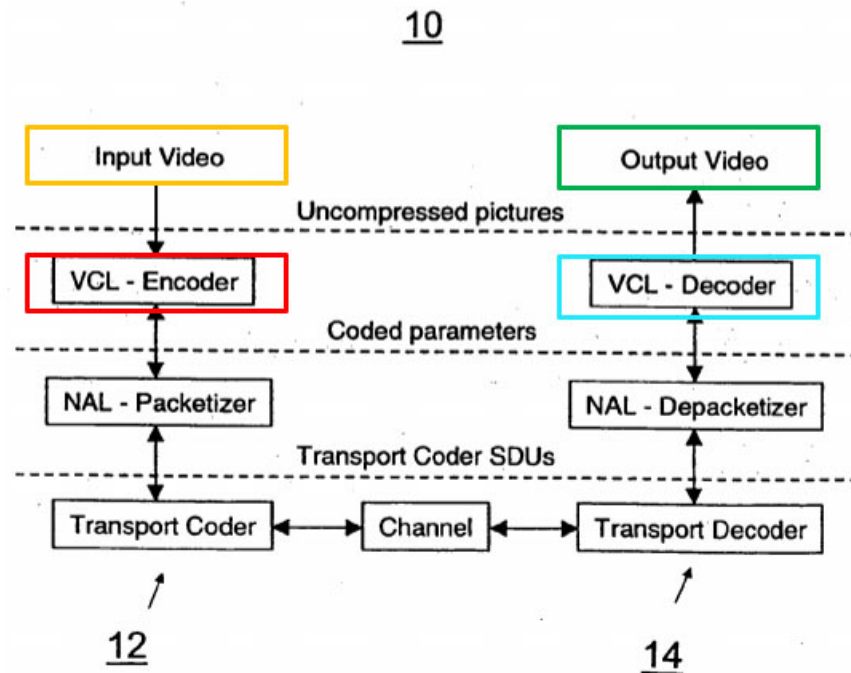
1. [1p] “A method for generating an encoded video signal from an original video signal, the original video signal comprising a sequence of video frames, the encoded video signal for use in a subsequent video display of said original video signal, the method comprising the steps of:”

Caglar teaches the preamble because *Caglar* discloses encoding video data such as picture sequences and encoding the input video (the claimed original video signal) for transmission from the encoder to a decoder to generate an output video (the claimed subsequent video display). Ex-1003, ¶65.

Caglar discloses an encoding procedure. For instance, *Caglar* discloses that “[t]he procedural steps presented in FIGS. 18 and 19 may be implemented in a video transmission system according to FIG. 16.” Ex-1005, ¶[0237]. *Caglar* discloses that procedure 18 is used to encode raw uncoded video data. *Id.*, FIG. 18a.

Caglar further discloses the claimed method for generating an encoded video signal from an original video signal because *Caglar* describes methods for “encoding a video signal.” *Id.*, Abstract, ¶¶[0103], [0111]. For example, *Caglar* discloses in Figure 16 below that an uncompressed video signal is encoded and

compressed to encode the input video. *Id.*, ¶¶[0009]; [0059]. Figure 16 shows video communications system 10 includes transmitter side 12 including a video coding layer (VCL) that encodes the input video. *Id.*, ¶[0059].



Id., FIG. 16.

Caglar also discloses the claimed original video signal comprising a sequence of video frames. For instance, *Caglar* discloses that FIG. 16 above is a “video communication system” and FIG. 16 shows the input video and output video as “[u]ncompressed pictures.” *Id.*, FIG. 16. A POSA would have understood that a series of pictures to make up a video would be in a sequence. Ex-1003, ¶68. This is consistent with what a POSA would have understood at the time, namely that a video is a series of images. *Id.*

Lastly, *Caglar* discloses the claimed encoded video signal for use in a subsequent video display of said original video signal because *Caglar* discloses that video communications system 10 includes receiver side 12 that receives a video bit-stream from transmitter side 10, and the video bit-stream is decoded and reconstructed into an “output video.” Ex-1005, ¶[0059], FIG. 16.

2. **[1A] “generating virtual reference data based on a portion of the original video signal, wherein the generated virtual reference data does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof;”**

Caglar teaches this claim limitation because *Caglar* discloses constructing a virtual reference frame (i.e. the claimed virtual reference data) based on a version of a first complete frame (i.e. the claimed portion of the original video signal), where the virtual reference frame is not to be displayed. Ex-1003, ¶70.

Caglar discloses the claimed generating virtual reference data based on a portion of the original video signal. For instance, *Caglar* discloses creating “a virtual reference frame.” Ex-1005, ¶[0243]. *Caglar* discloses, “*defining a first virtual frame on the basis of a version of the first complete frame*” or a second complete frame. *Id.*, ¶[0105] (emphasis added); *see id.*, ¶¶[0109], [0113], [0115], [0122], [0138], [0145], [0172], [0191], [0195]. Additionally, *Caglar* discloses “a chain of virtual frames is constructed using the higher importance information of the encoded video frame.” *Id.*, ¶[201]. *Caglar* further discloses that the creation of

the virtual frame in its encoding method with respect to FIG. 18. *Caglar* discloses that FIG. 18 “illustrates an encoding procedure according to the invention.” *Id.*, ¶[0229]. And, as discussed above, FIG. 18 is implemented in a video transmission system according to FIG. 16. *Id.*, ¶[0237]. **Step 116** corresponds to receiving “uncompressed pictures,” discussed above and shown in FIG. 16. Ex-1003, ¶72. **Step 116** of FIG. 18 includes receiving “raw uncoded video data for a frame.” Ex-1005, FIG. 18, ¶[0238]. This raw uncoded video data corresponds to the claimed “original video signal.” Ex-1003, ¶72.

Caglar further discloses the claimed construction of the reference data. After receiving the uncoded video data, *Caglar* discloses that its FIG. 18 encoding procedure includes coding an INTER frame in **step 132**. Ex-1005, ¶[0240]. *Caglar* discloses receiving “an indication of a frame to be used as a reference in encoding the current frame in INTER frame format” in **step 134**. *Id.*, ¶[0240]. In **step 140** “[t]he identified reference frame may be a complete frame or a virtual frame and so the encoder determines whether a virtual reference is to be used.” *Id.* And then, in **step 142**, “[i]f a virtual reference frame is to be used, it is retrieved from the virtual reference frame buffer.” *Id.*, ¶[0241]. In **steps 160 and 162**, *Caglar* discloses the virtual frame is stored in the buffer once decoded from the current frame “in order to form a reconstruction of a virtual frame.” *Id.*, ¶[0241] (emphasis added).

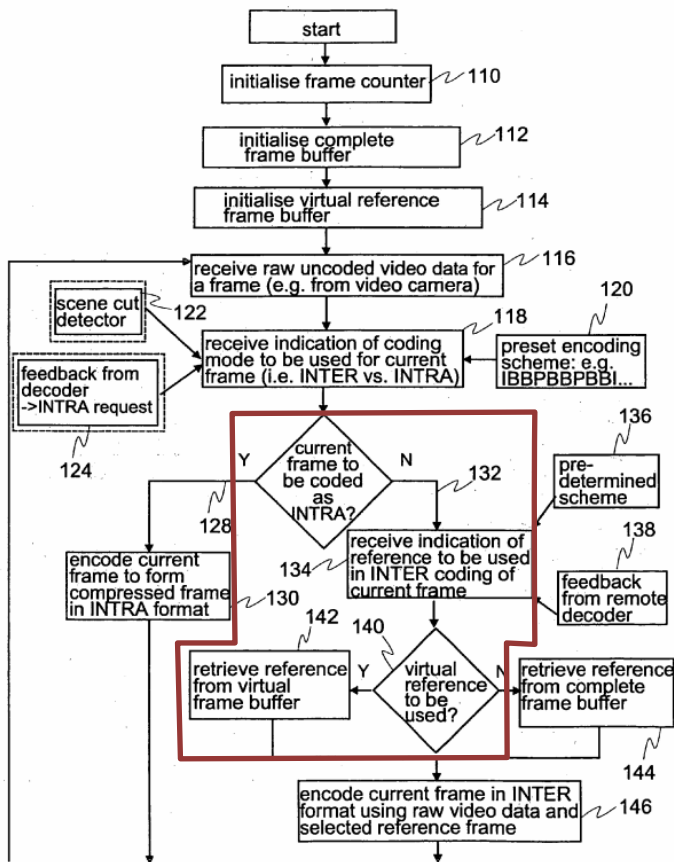


Fig. 18a

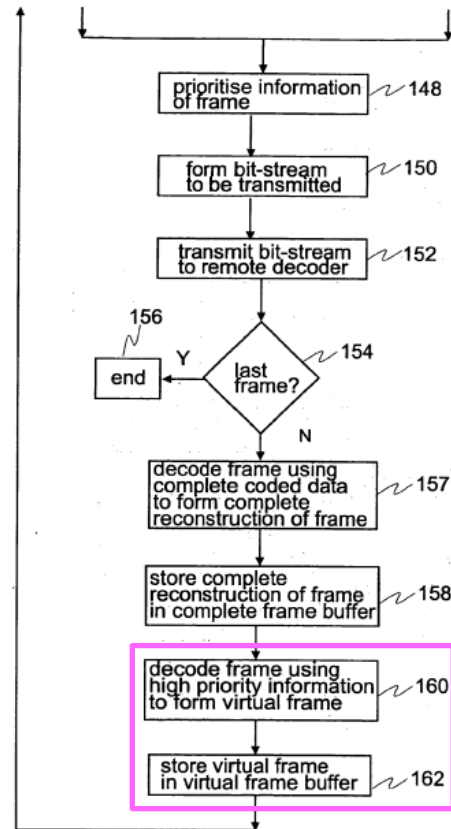


Fig. 18b

(Left) *Caglar*, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

Caglar's virtual reference frame discloses both the Petitioners and Patent Owners constructions of "virtual reference" for the '960 patent because *Caglar* discloses that its "virtual frame is not displayed." *Id.*, ¶[0127]. Further, *Caglar* discloses "virtual frames are generally not intended to be displayed." *Id.*, ¶[0201]; *see id.*, ¶[0210], [0271]. The construction of "virtual reference" adopted for this IPR is "a group of pixels (e.g., a block) that is used as reference material for encoding portions of the video signal (e.g., a motion-compensated inter-predicted block), but that does not comprise or represent any portion of the actual video

sequence to be displayed.” *Caglar*’s virtual frame meets this definition because *Caglar*’s virtual frame is for the encoding and decoding of a complete frame, but the virtual frame is not to be displayed. Ex-1003, ¶74. If the Board determines that “virtual reference” should be construed under its plain and ordinary meaning, *Caglar* discloses it because *Caglar* discloses a “virtual reference frame.” Ex-1003, ¶74.

Caglar discloses the claimed “generated virtual reference data does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof.” *Caglar* discloses the virtual frame is not to be displayed. Ex-1005, ¶[0201]; *see id.*, ¶¶[0210], [0271].

To the extent Patent Owner argues that the claimed generated virtual reference data is not constructed based on information from a complete frame, *Caglar* discloses that its virtual frames may be constructed on the basis of a previous virtual frame. *Caglar* discloses that its decoder may use a “newly constructed virtual frame . . . for use in connection with the reconstruction of a *subsequent* complete or *virtual frame*.” *Id.*, ¶[0247] (emphasis added). Thus, *Caglar* discloses that the constructed virtual frame “does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof.”

3. [1B] “encoding, using a processor, said generated virtual reference data and incorporating said encoded virtual reference data into the encoded video signal;”

Caglar teaches this claim limitation because it claims a method of encoding, with a microprocessor (the claimed processor), the virtual reference frame (i.e. generated virtual reference data) and forming a bit-stream (i.e. the claimed incorporating) including the virtual reference frame in a bit-stream for transmission to a decoder. Ex-1003, ¶77.

Caglar discloses the claimed processor. *Caglar* discloses the encoding procedure of FIG. 18 is “executed on a general purpose microprocessor or dedicated signal processor (DSP).” Ex-1005, ¶[0262].

Caglar discloses the claimed encoding generated virtual reference data. *See also* Section **Error! Reference source not found.** For instance, *Caglar* discloses that once the virtual reference frame is selected, in [step 146](#), the frame is encoded in INTER format and includes the raw video data and the selected reference frame. *Id.*, FIG. 18a, ¶[0241]. The selected reference frame can be a virtual frame. *Id.*, ¶[0259]. This is shown in FIG. 18 below.

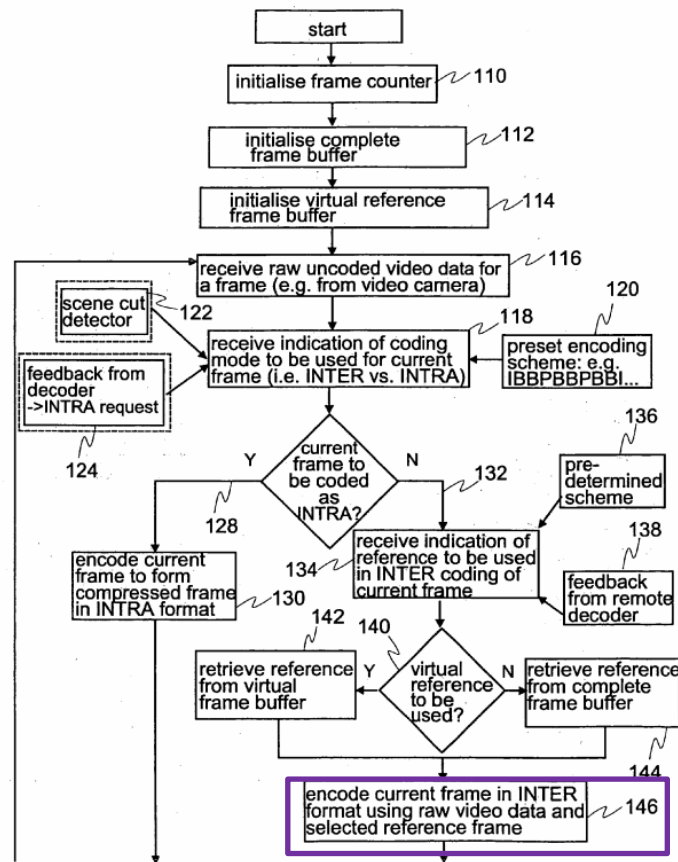


Fig. 18a

Ex-1005, Annotated Fig. 18a.

Caglar discloses the claimed incorporating said encoded virtual reference data into the encoded video signal. For instance, *Caglar* discloses that the encoded frame, including the virtual reference frame, is included in a bit-stream for transmission from the encoder to the decoder. *Id.*, ¶[0242]. *Caglar* discloses that the bit-stream “is arranged in a hierarchical structure with four layers which are, from top to bottom, a picture layer, a picture segment layer, a macroblock (MB) layer, and a block layer.” *Id.*, ¶[0019]. The bit-stream is formed in [step 150](#), shown below in FIG. 18b. *Id.*, ¶[0242].

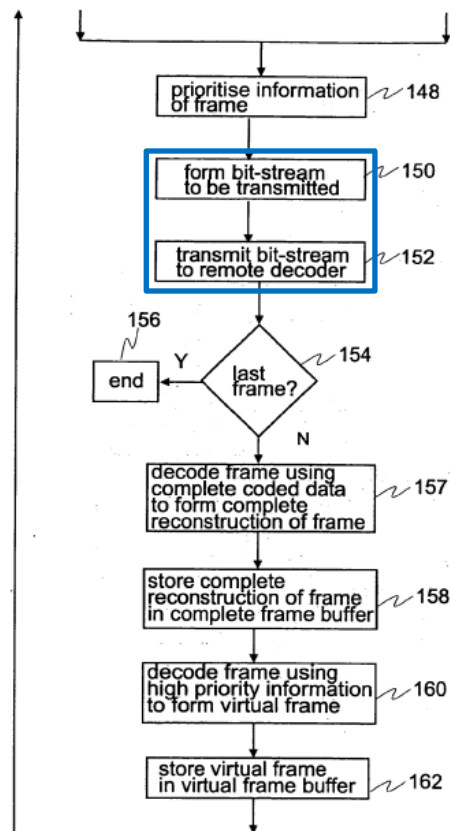


Fig. 18b

Id., Annotated Fig. 18b.

Further, as part of the claimed incorporation, *Caglar* also discloses that “the [signaling from the encoder to the decoder] may apply to a part of a picture, for example a slice, a block, a macroblock or a group of blocks.” *Id.*, ¶[0130]. This signalling in the bit-stream includes the raw video data and the selected virtual reference frame. *Id.*, ¶¶[0241]-[0242]; Ex-1003, ¶81.

To the extent Patent Owner argues that forming a hierarchical structure like blocks for a bit-stream, as disclosed by *Caglar*, does not disclose “incorporating said encoded virtual reference data into the encoded video signal,” *Duvivier*

discloses it. *Duvivier* discloses method 800 that describes a process for forming a macroblock. Ex-1006, ¶[0055]. As part of forming the macroblock, [step 810](#) allocates a portion of the storage structure for “storing data of the slice,” where the slice is of a video frame, and, in [step 813](#), the method includes storing “additional useful/meaningful data” including “reference frame index data.” FIG. 8 is shown below.

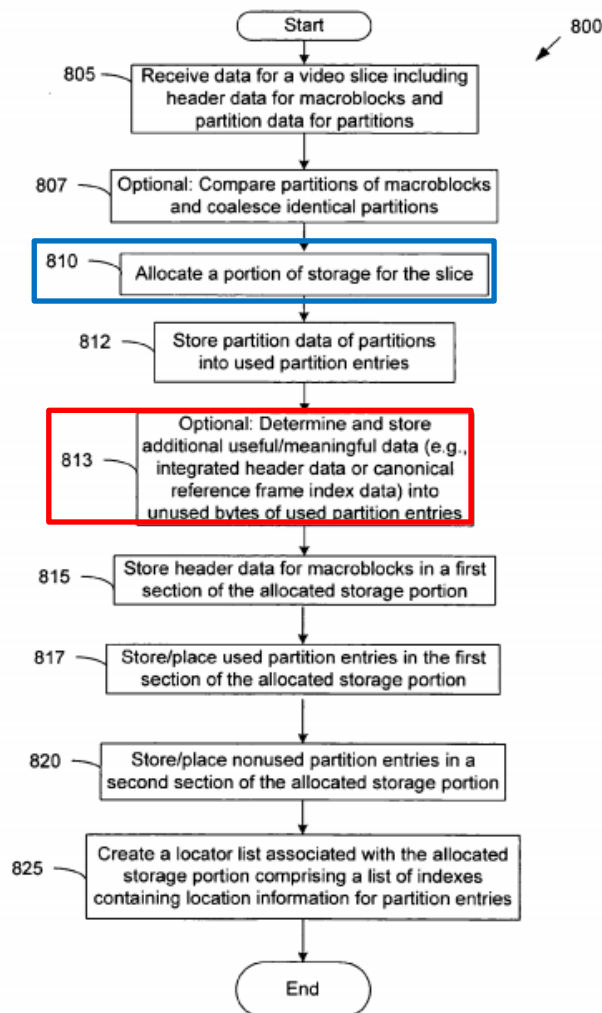


Figure 8

Id., Annotated FIG. 8.

Thus, the combination of *Caglar* and *Duvivier* renders obvious this claim limitation. Ex-1003, ¶83.

i. A POSA Would Have Combined *Caglar* and *Duvivier*

First, A POSA would have sought to combine *Duvivier*'s teachings with that of *Caglar*. A POSA would have understood that the bit-stream disclosed by *Caglar* would have included forming a macroblock—as taught by *Duvivier*—with uncoded video data and the selected virtual reference frame, for example, as disclosed above in Sections VII.A.1-3. Ex-1003, ¶84. *Duvivier* discloses that its system is more efficient for the transmission of video data, Ex-1006, ¶¶[0002], [0021], [0045], and thus a POSA would have been motivated to modify *Caglar* to achieve that efficiency. Ex-1003, ¶84. Further, a POSA would have understood that partitioning of the uncoded video data, as taught by *Duvivier*, and the selected virtual reference frame would have been important to reduce the bandwidth of *Caglar*'s bit-stream. *Id.* The efficiency is achieved through the use of a storage structure that allows for the “efficient use of . . . encoding and decoding of video data streams.” *Id.* (quoting Ex-1006, Title, ¶¶[0021], [0045]-[0048]).

Second, and alternatively, a POSA would have been motivated to modify *Caglar* with *Duvivier*. *Duvivier* discloses that its system is more efficient for the transmission of video data. Ex-1006, ¶¶[0021], [0045]-[0048]; Ex-1003, ¶85. Thus, a POSA would be further motivated to include *Duvivier*'s formation of the video

bit-stream by forming a macroblock from *Caglar*'s uncoded video data and the selected virtual reference frame because *Duvivier*'s methods enables forming a block with reference data and data for a video frame. Ex-1003, ¶85.

A POSA would have found reason to partition *Caglar*'s uncoded video data and the selected virtual reference frame to achieve the greatest efficiency possible to reduce the amount of bandwidth of the bitstream transmission. Ex-1003, ¶86. Further, a POSA would have recognized that such an implementation would have been a common sense and predictable design choice because *Caglar* describes forming a bitstream (i.e. a video data stream) from an encoder to a decoder, and *Duvivier* discloses the "efficient use of storage in the encoding and decoding of video data streams." *Id.* (citing Ex-1006, Title, ¶¶[0021], [0045]-[0048]). A POSA would have had a reasonable expectation of success in the implementation because both *Caglar* and *Duvivier* are directed towards video data transmission between an encoder and a decoder according to well-known coding standards such as H.263. Ex-1003, ¶86 (citing Ex-1007, 10; Ex-1008, 574).

4. **[1C] “incorporating into the encoded video signal an indication that said encoded virtual reference data incorporated therein comprises data which does not represent any portion of any individual frame of the original video signal to be displayed in said subsequent video display thereof;”**

Caglar teaches this claim limitation because it discloses encoding into the current frame (the claimed “incorporating”) a bit-stream using a header (the claimed “indication that said encoded virtual reference data incorporated therein”) that indicates whether the complete frame uses a virtual reference frame. Ex-1003, ¶87.

First, *Caglar* discloses the claimed indication. For instance, *Caglar* discloses that its “*pictures are encoded* in such a way that they comprise picture headers.” Ex-1005, ¶[0276]. (emphasis added). Specifically, *Caglar* discloses the header includes “a particular value is included to indicate whether the picture uses one or more virtual references frames.” *Id.*

Next, *Caglar* discloses the claimed incorporating an indication. For instance, *Caglar* discloses forming a bit-stream with the header. *Caglar* discloses that the encoded pictures have headers. *Id.*, ¶[0276]. As illustrated in FIG. 18, the frame is encoded in step 146 before the bit-stream is formed in step 150. *Id.*, FIG. 18a. Thus, a POSA would have understood that forming the bit-stream includes the header. Ex-1003, ¶89.

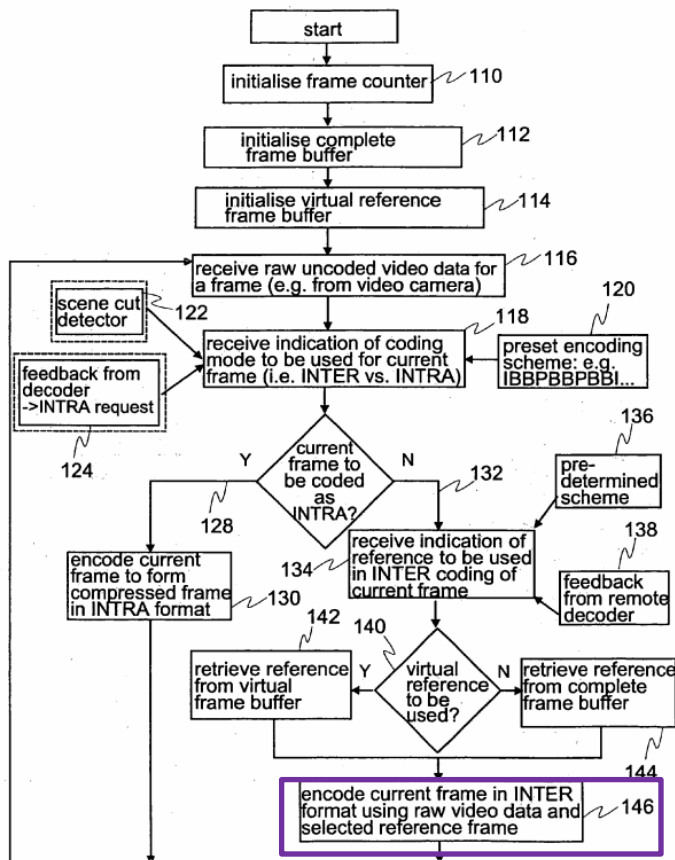


Fig. 18a

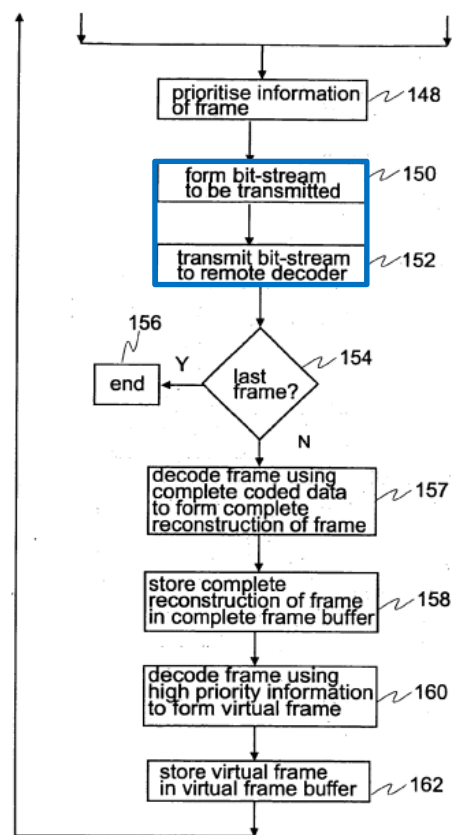


Fig. 18b

(Left) Ex-1005, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

Lastly, *Caglar* discloses the claimed indication that said encoded virtual reference data incorporated therein “comprises data which does not represent any portion of any individual frame of the original video signal to be displayed in said subsequent video display thereof.” As discussed above in Section VII.2, *Caglar* discloses that its virtual frames are not to be displayed. *Id.*, ¶¶[0201], [0210], [0271]. To the extent Patent Owner argues that the claimed generated virtual reference data is not constructed based on information from a complete frame,

Caglar discloses that the virtual frame may be constructed on the basis of a previous virtual frame as discussed above in Section VII.2.

To the extent Patent Owner argues that forming a hierarchical structure like blocks for a bit-stream does not disclose “incorporating said encoded virtual reference data into the encoded video signal,” *Duvivier* discloses it. *Duvivier* discloses method 800 that describes a process for forming a macroblock. Ex-1006, ¶[0055]. As part of forming the macroblock, [step 810](#) allocates a portion of the storage structure for “storing data of the slice,” where the slice is of a video frame, and, in [step 813](#), the method includes storing “additional useful/meaningful data” including “reference frame index data.” And, [step 815](#) includes storing “header data for each macroblock.” *Id.*, ¶[0056]. FIG. 8 is shown below.

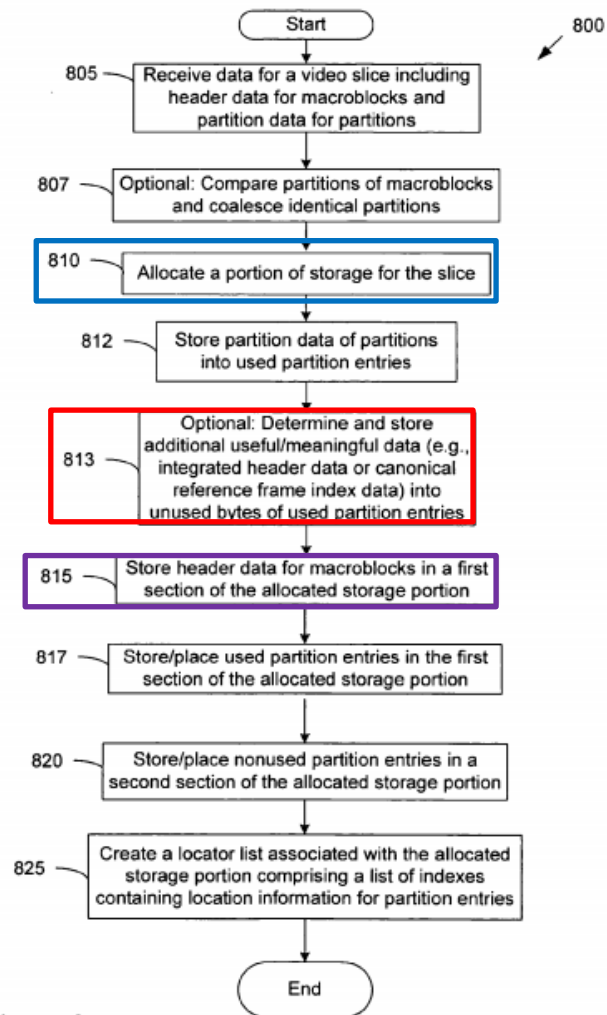


Figure 8

Id., Annotated FIG. 8.

A POSA would have found claim 1 obvious based on *Caglar* and *Duvivier*. Ex-1003, ¶92. And, a POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. *Id.*

5. [1D] “encoding, using a processor, one or more portions of the original video signal which are to be displayed in said subsequent video display thereof, wherein said encoding of said one or more portions of said original video signal which are to be displayed are based on and specifically reference a portion of said encoded virtual reference data; and”

Caglar teaches this claim limitation because teaches a microprocessor (i.e. the claimed processor) for encoding the video signal to include the uncoded video data (i.e. the claimed one or more portions of the original video signal) to form a complete frame (i.e. the claimed one or more portions of the original video signal which are to be displayed in said subsequent video display thereof), where the encoding of the complete frame is based on a virtual reference frame that includes a header (the claimed “said encoded virtual reference data”) that refers to the virtual reference frame. Ex-1003, ¶93.

Caglar discloses the claimed processor. *Caglar* discloses the encoding procedure of FIG. 18 is “executed on a general purpose microprocessor or dedicated signal processor (DSP).” Ex-1005, ¶[0262].

Caglar discloses the claimed encoding one or more portions of the original video signal because *Caglar* discloses, in [step 146](#), that “[t]he current frame is then encoded in INTER frame format *using the raw video data and the selected reference frame.*” *Id.*, ¶[0241] (emphasis added). This is shown in FIG. 18a below.

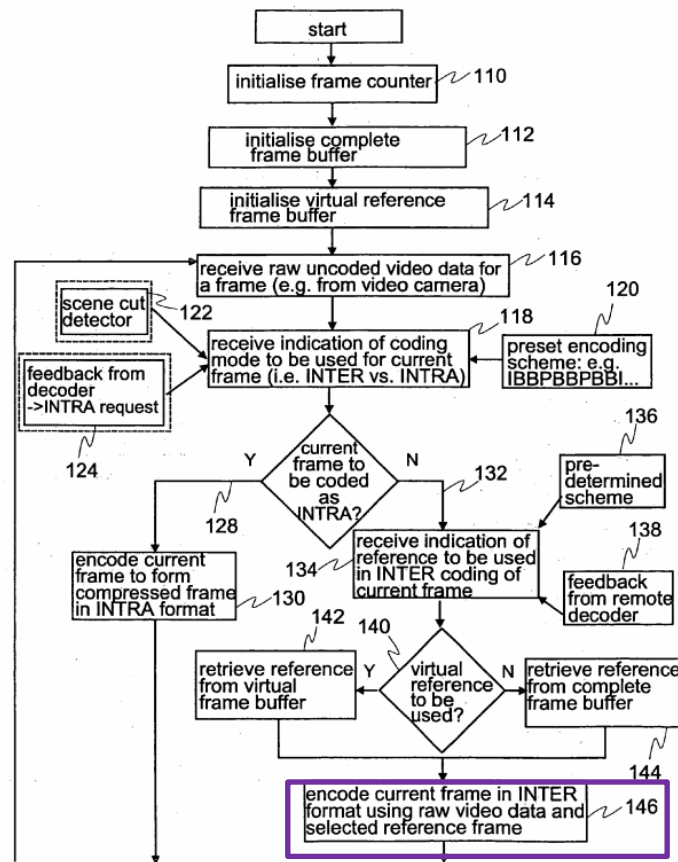


Fig. 18a

Ex-1005, Annotated Fig. 18a.

Caglar discloses the claimed “said encoding of said one or more portions of said original video signal which are to be displayed.” *Caglar* discloses encoding a complete frame, and that a complete frame is “complete in the sense that an image capable of display can be formed.” *Id.*, ¶¶[0110], [0118].

Caglar discloses the claimed encoding of said one or more portions of said original video signal “are based on and specifically reference a portion of said encoded virtual reference data.” *Caglar* discloses that a second complete frame is sent to the decoder using a bit-stream “comprising information for use in

reconstruction of the second complete frame such that the second complete frame can be reconstructed *on the basis of the first virtual frame.*” *Id.*, ¶[0106] (emphasis added). When received by the decoder, “[t]he decoder then determines whether the current frame is encoded in INTRA frame format or INTER frame format (step 216). This can be determined from information received, for example, in the picture header.” *Id.*, ¶[0246]. The header includes “a particular value is included to indicate whether the picture uses one or more virtual reference frames.” *Id.*, ¶[0276].

6. [1E] “incorporating said encoded portions of said original video signal which are to be displayed into said encoded video signal.”

Caglar teaches this claim limitation because it claims forming a macroblock (i.e. the claimed incorporating) including the header and the complete frame (i.e. the claimed encoded portions of the original video signal which are to be displayed) to transmit from the encoder to the decoder. Ex-1003, ¶98.

Caglar discloses the claimed “incorporating said encoded portions of said original video signal which are to be displayed into said encoded video signal” because it discloses forming a macroblock that includes the encoded original video with the header indicating the virtual reference frame. *Caglar* discloses, in [step 146](#), that “[t]he current frame is then encoded in INTER frame format *using the raw video data* and the selected reference frame.” Ex-1005, ¶[0241] (emphasis

added). Then, in [step 150](#), the bit-stream is formed for transmission to the decoder, *id.*, FIG. 18b, including that the bit-stream “is arranged in a hierarchical structure with four layers which are, from top to bottom, a picture layer, a picture segment layer, a macroblock (MB) layer, and a block layer.” *Id.*, ¶[0019]. Steps 146, 150, and 152 are shown in FIG. 18 below.

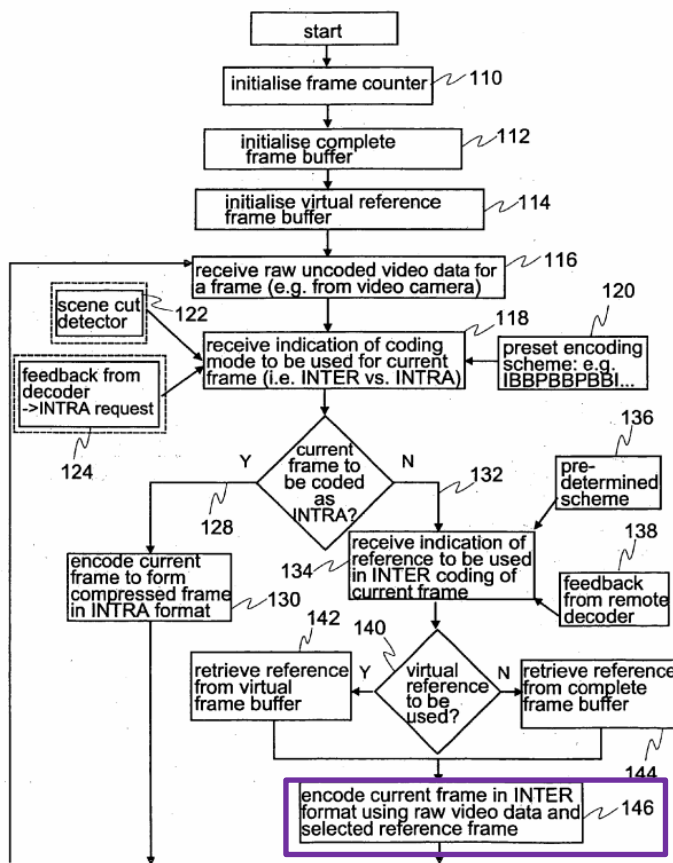


Fig. 18a

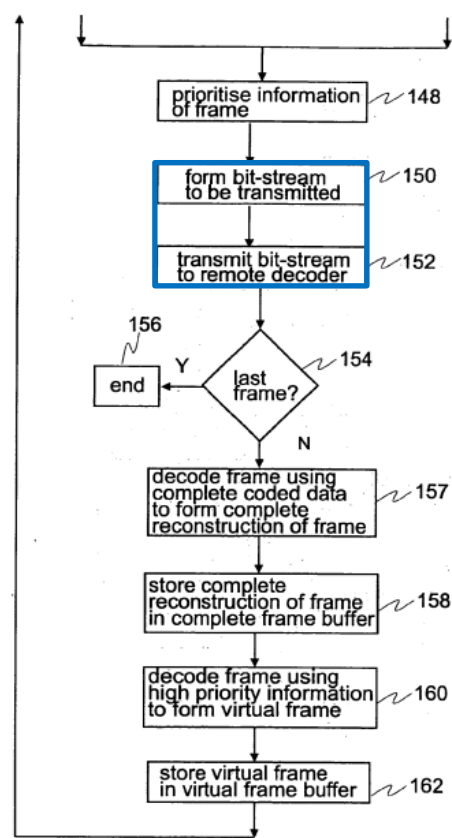


Fig. 18b

(Left) Ex-1005, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

Caglar discloses the claimed encoding of said one or more portions of said original video signal “are based on and specifically reference a portion of said encoded virtual reference data.” *Caglar* discloses that a second complete frame is

sent to the decoder using a bit-stream “comprising information for use in reconstruction of the second complete frame such that the second complete frame can be reconstructed *on the basis of the first virtual frame.*” *Id.*, ¶[0106] (emphasis added). When received by the decoder, “[t]he decoder then determines whether the current frame is encoded in INTRA frame format or INTER frame format (step 216). This can be determined from information received, for example, in the picture header.” *Id.*, ¶[0246]. The header includes “a particular value is included to indicate whether the picture uses one or more virtual reference frames.” *Id.*, ¶[0276]. *Caglar* discloses that the picture header is “included in slice headers, macroblock headers and/or block headers, depending on the kind of packetization used.” *Id.*

To the extent Patent Owner argues that forming a hierarchical structure like blocks for a bit-stream does not disclose “said encoded portions of said original video signal which are to be displayed into said encoded video signal,” *Duvivier* discloses it. *Duvivier* discloses method 800 that describes a process for forming a macroblock. Ex-1006, ¶[0055]. As part of forming the macroblock, [step 810](#) allocates a portion of the storage structure for “storing data for a slice of a video frame.” *Id.*, ¶[0030]. FIG. 8 is shown below.

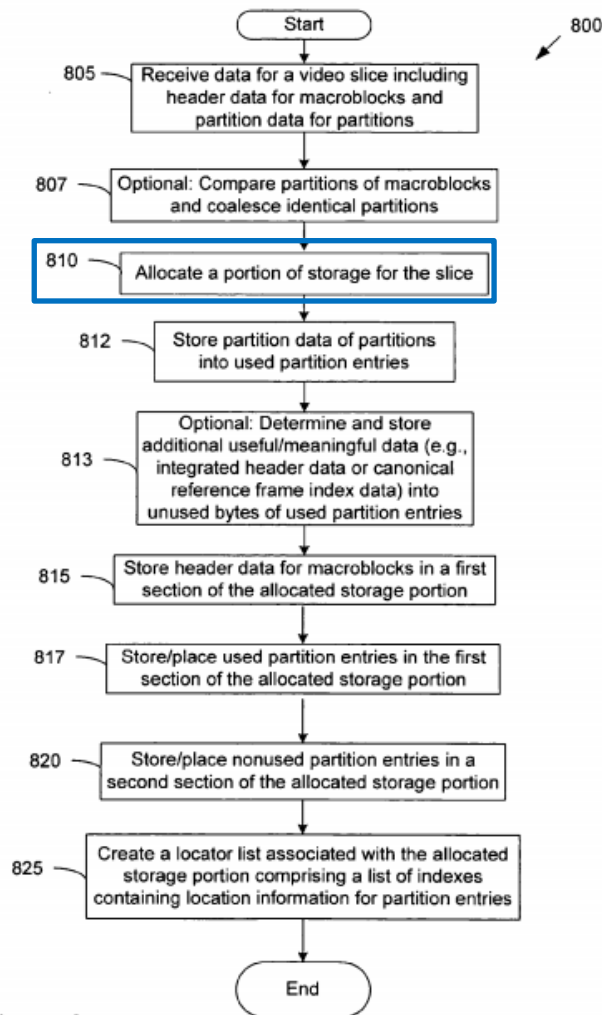


Figure 8

Id., Annotated FIG. 8.

A POSA would have found claim 1 obvious based on *Caglar* and *Duvivier*. Ex-1003, ¶102. And, a POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. *Id.*

- B. [Claim 2] “The method of claim 1 wherein said encoded video signal comprises a block-based encoding of said original video signal, wherein said virtual reference data comprises one or more virtual reference blocks, and wherein said encoded portions of said original video signal which are to be displayed are encoded**

based on said encoded virtual reference data with use of a block-based motion compensated prediction scheme.”

Caglar teaches this claim because it discloses encoding blocks (the claimed “block-based coding”) to form a bit-stream, including encoding a current frame based on a virtual reference frame and raw video data, and where the encoded current frame is to be displayed and is encoded based on the virtual reference frame (the claimed “virtual reference data”) using motion compensation prediction. Ex-1003, ¶103.

The ’960 patent states that “[m]ost major standard video codecs (i.e., coders and decoders) achieve a data compression advantage over still image coding techniques by using a block-based, motion-compensated prediction scheme. Such schemes are fully familiar to those of ordinary skill in the art.” Ex-1001, 1:15-23.

Caglar discloses the claimed “said encoded video signal comprises a block-based encoding of said original video signal,” because *Caglar* discloses that, “[a]ccording to H.263, pictures are assembled into macroblocks (MBs).” Ex-1005, ¶¶[0018]-[0019]. This block coding is used in the procedures disclosed by *Caglar*. *Id.*, ¶[0200]. Specifically, *Caglar* discloses that the bit-stream from the encoder to the decoder “may apply to a part of a picture, for example a slice, a block, a macroblock or a group of blocks.” *Id.*, ¶[0156]; *see id.*, ¶[0263].

Caglar discloses the claimed “said virtual reference data comprises one or more virtual reference blocks,” because *Caglar* discloses references to frames in *Caglar* are also references to blocks or macroblocks “within a frame.” *Id.*, ¶¶[0156], [0198]; *see id.*, ¶[0263]. *Caglar*’s step 146 includes encoding the current frame using raw video data and a virtual reference frame. *Id.*, ¶[0241]. A POSA would have understood the virtual reference frame would include blocks or macroblocks within a frame. *Id.*, ¶[0198]; Ex-1003, ¶106.

Caglar discloses the claimed “encoded portions of said original video signal which are to be displayed are encoded based on the encoded virtual reference data.” *Caglar* discloses, in step 146, that “[t]he current frame is then encoded in INTER frame format *using the raw video data* and the selected reference frame.” *Id.*, ¶[0241] (emphasis added).

Caglar discloses the claimed “said encoded portions of said original video signal encoded based on a block-based motion compensated prediction scheme.” *Caglar* discloses “motion compensated predictions in which an alternative prediction path generated using virtual frames is used.” *Id.*, ¶[0201]. Further, “the use of virtual frames according to the invention is a method of shortening prediction paths in motion compensated prediction.” *Id.*, ¶[0205]. Steps 142 and 146 of FIG. 18a include encoding complete frames using a virtual reference frame

for “motion compensated prediction.” *Id.*, ¶[0281]. *Caglar* discloses that its disclosure of encoding frames may applies to blocks. *Id.*, ¶¶[0156], [0198], [0263]. *Duvivier* discloses that a bitstream is created during the encoding process. Ex-1006, ¶[0009]. *Duvivier* discloses [a] video stream is comprised of a sequence of video frames where each frame is comprised of multiple macroblocks.” *Id.*, ¶[0004]. Further, [a] video codec encodes each frame in the sequence by dividing the frame into one or more slices or sub-portions, each slice containing an integer number of macroblocks.” *Id.*, ¶[0004]. Because *Caglar* discloses a video encoding method that forms a bit-stream, a POSA would have understood that *Caglar* would have used a block-based encoding procedure like that disclosed in *Duvivier*. Ex-1003, ¶109. A POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. *Id.*

C. [Claim 6] “The method of claim 2 wherein said encoded virtual reference data and one encoded portion of said original video signal which is to be displayed are incorporated into said encoded video signal together as an encoded dual block.”

Caglar teaches this claim because it discloses using encoding a virtual reference frame and raw uncoded video data along with a header, and that this method would be implemented on blocks. Ex-1003, ¶110.

The ’960 patent describes a dual block as “composed of three parts: a header, a primary block and a secondary block.” Ex-1001, 5:48-50. The primary

block comprises “the encoding of a virtual reference block.” *Id.*, 5:61-64. The secondary block comprises “encoding of the actual block.” *Id.*, 5:64-6:2. The header “is a flag indicating the type of reference to follow.” *Id.*, 5:50-51.

As discussed above in Section VII.2, *Caglar* discloses encoding the current frame based on the raw video data (i.e. claimed one encoded portion of said original video signal which is to be displayed) and the selected virtual reference frame (i.e. claimed virtual reference data) in step 146. Further, *Caglar* discloses encoding a header. Ex-1005, ¶[0276]. *Caglar* discloses these steps, shown in FIG. 18, applies to subsets of frames such as blocks. *Id.*, ¶¶[0156], [0198]; *see id.*, ¶[0263]. The encoded information is then formed into a bit-stream (i.e. claimed video signal) in step 150. *Id.*, ¶[0242]; FIG. 18b.

To the extent Patent Owner argues that *Caglar* does not disclose incorporating the raw video data and selected virtual reference frame into an encoded block, *Duvivier* discloses it. *Duvivier*, discloses forming a macroblock including a video slice, reference frame index data, and header data. *Duvivier* discloses “[a] video codec encodes each frame in the sequence by dividing the frame into one or more slices or sub-portions, each slice containing an integer number of macroblocks.” Ex-1006, ¶[0004]. *Duvivier* discloses “coalescing partitions of macroblocks of a video slice.” *Id.*, ¶[0095]. For forming the macroblock, [step 810](#) allocates a portion of the storage structure for “storing data

of the slice,” where the slice is of a video frame, and, in **step 813**, the method includes storing “additional useful/meaningful data” including “reference frame index data.” *Id.*, ¶[0058]. And, step **815** includes storing “header data for each macroblock.” *Id.*, ¶[0056]. FIG. 8 is shown below.

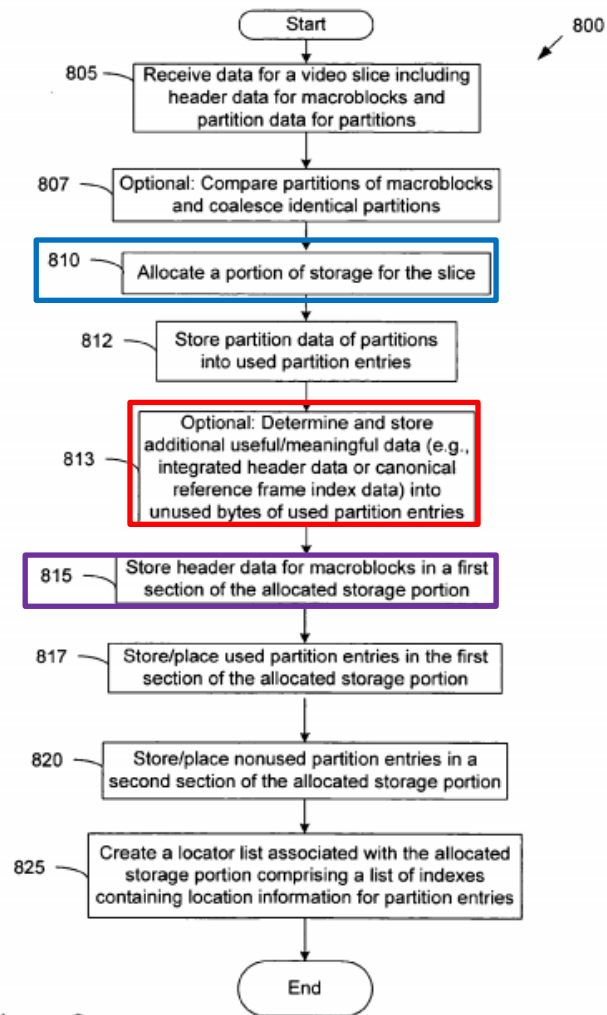


Figure 8

Id., Annotated FIG. 8.

A POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. Ex-1003, ¶113.

D. [Claim 7] “The method of claim 6 wherein the encoded dual block further comprises a motion vector representative of a relocation within a video frame that is to be associated with the encoded virtual reference data incorporated in the encoded dual block.”

Duvivier teaches this claim because it discloses that motion vector information is included in the macroblock. Ex-1003, ¶114.

Duvivier discloses the claimed “encoded dual block further comprises a motion vector.” *Duvivier* discloses “[t]he data for the slice includes partition data (e.g., motion vector and reference frame index data) associated with partitions of the macroblocks of the slice and header data for each macroblock.” Ex-1006, ¶[0053].

Duvivier discloses the claimed “motion vector representative of a relocation within a video frame.” *Duvivier* discloses that the predictive information that is derived is “a motion vector (comprised of x and y components) and an associated indicated to a frame (in a sequence of frames) that the motion vector is based upon.” *Id.*, ¶[0009]. A POSA would have understood that the motion vector including x and y components that is based on a frame would indicate a relocation of a partition. Ex-1003, ¶116. The partition is part of the video slice, and thus the relocation is within a video frame. *Id.*

Duvivier discloses the claimed motion vector “that is to be associated with the encoded virtual reference data incorporated in the encoded dual block.”

Duvivier discloses that “[a] reference frame index [is] associated with a motion vector.” Ex-1006, ¶[0011]. A POSA would have understood that the reference frame index would indicate a virtual reference frame. Ex-1003, ¶117. A POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. Ex-1003, ¶117.

E. [Claim 8]

1. **[8A] “The method of claim 1 wherein the encoded video signal comprises a block-based encoding of said original video signal, wherein one of said portions of the original video signal which is to be displayed is comprised in a given frame of said original video signal,**

Caglar teaches this claim because it discloses using block-based encoding to encode the bit-stream, including the first complete frame, and where the virtual frame includes a virtual reference block, and where the encoded second complete frame is to be displayed and is encoded based on the first virtual frame using a motion compensation. Ex-1003, ¶118.

Caglar discloses the claimed “said encoded video signal comprises a block-based encoding of said original video signal,” because *Caglar* discloses that, “[a]ccording to H.263, pictures are assembled into macroblocks (MBs).” Ex-1005, ¶¶[0018]-[0019]. This block coding is used in the procedures disclosed by *Caglar*. *Id.*, ¶[0200]. Specifically, *Caglar* discloses that the bit-stream from the encoder to

the decoder “may apply to a part of a picture, for example a slice, a block, a macroblock or a group of blocks.” *Id.*, ¶[0156]; *see id.*, ¶[0263].

Caglar discloses the claimed “one of said portions of the original video signal which is to be displayed is comprised in a given frame of said original video signal,” because *Caglar* discloses a block may be of a complete frame, where the complete frame is meant to be displayed. *Id.*, ¶¶[0110], [0118]; Ex-1003, ¶¶119-120.

2. **[8B] wherein said virtual reference data is generated based on said given frame of said original video signal, and wherein said one of said portions of the original video signal which is to be displayed is encoded based on said encoded virtual reference data with use of an intra-coding prediction scheme.”**

Caglar teaches this claim because it discloses a virtual reference frame based on a frame such as a first complete frame, and where the complete frame, which is to be displayed, is encoded based on the virtual reference frame and with use of an intra-coding prediction scheme. Ex-1003, ¶121.

Caglar discloses the claimed “virtual reference data is generated based on said given frame of said original video signal.” *Caglar* discloses a video sequence of frames I0, P1, P2, and P3 shown in FIG. 21. Frame I0 is an intra-coded frame. Ex-1005, ¶[0272]. As illustrated, “virtual frame I0’ is generated from a part of the bit-stream corresponding to frame I0.” *Id.*

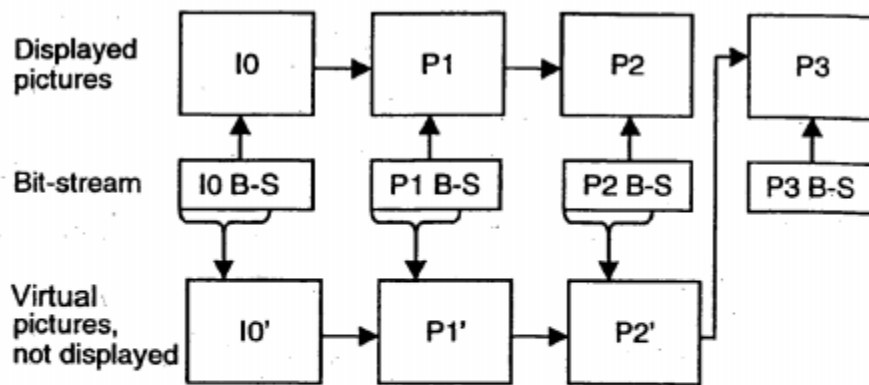


Fig. 21

Id., FIG. 21.

Caglar discloses the claimed “wherein said one of said portions of the original video signal which is to be displayed is encoded based on said encoded virtual reference data with use of an intra-coding prediction scheme.” *Caglar* discloses “artificial frame P1 is generated using I0’ as a reference for motion compensated prediction, together with part of the bit-stream for P1.” *Id.* In this case, frame P1 is to be displayed. *Id.*, FIG. 21. Frame P1 is generated using a virtual frame, I0’, as a reference where I0’ is based on an intra-coded frame. Accordingly, a POSA would have understood that frame P1, a frame that is displayed, is encoded based on a virtual reference frame (i.e. claimed virtual reference data) and with use of an intra-coded frame (i.e. intra-coding prediction scheme). Ex-1003, ¶123.

F. Claim 9

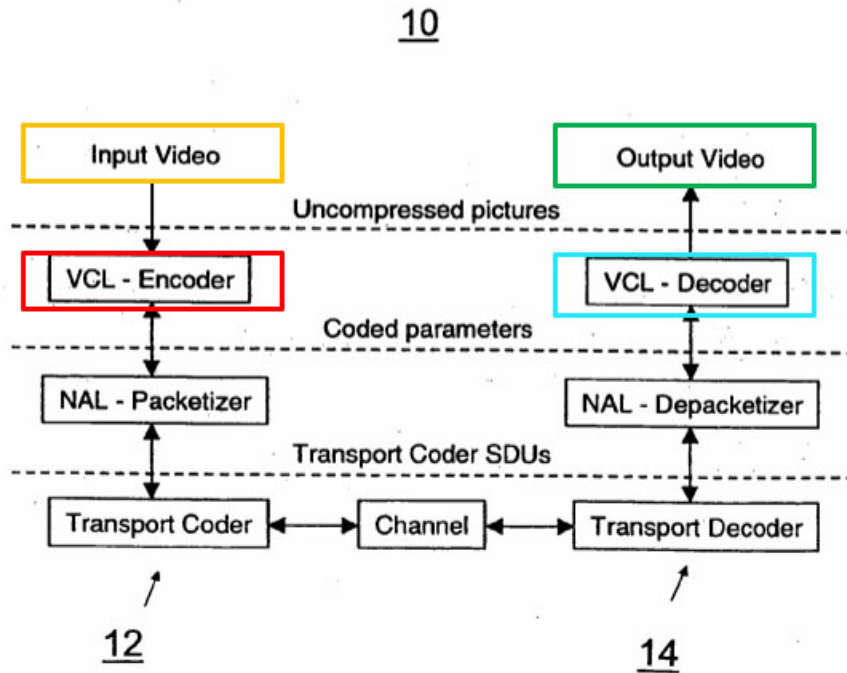
1. [9p] **“A method for decoding an encoded video signal to generate a decoded video signal for use in a subsequent video display of an original video signal, the original video signal comprising a sequence of video frames, the encoded video signal having been generated from the original video signal, the method comprising the steps of:”**

Caglar teaches this claim limitation because it discloses decoding an encoded input video (the claimed “original video signal”) to decode and reconstruct an output video (the claimed “decoded video signal for use in a subsequent video display of an original video signal”), where the input video is a series of frames and the encoded video signal is generated from the input video. Ex-1003, ¶124.

Claim 9 recites “a method for decoding an encoded video signal” where claim 1 recites “a method for generating an encoded video signal.”

Caglar discloses the claimed “method for decoding an encoded video signal to generate a decoded video signal for use in a subsequent video display of an original video signal,” because *Caglar* describes methods for “decoding and reconstruction of the image data” from an encoder. *Id.*, Abstract, ¶[0059]. For example, *Caglar* discloses in Figure 16 below that shows an uncompressed video signal is encoded and compressed to create an encoded video signal that is then

decoded and reconstructed. Ex-1005, ¶[0059]. The result of decoding and reconstruction is an output video. *Id.*, FIG. 16.



Id., FIG. 16.

Caglar discloses FIG. 19 that “illustrates a decoding procedure according to the invention.” *Id.*, ¶[0230]. FIG. 19 is “implemented in a video transmission system according to FIG. 16.” *Id.*, ¶[0237].

Caglar discloses the claimed original video signal comprising a sequence of video frames as discussed above in Section VII.1 because *Caglar* discloses an input video comprising a sequence of frames. Ex-1003, ¶128.

Caglar discloses the claimed “the encoded video signal having been generated from the original video signal” because *Caglar* discloses *Caglar*

describes methods for “encoding a video signal” from an input video. Ex-1005, ¶[238]; FIG. 16. For example, *Caglar* discloses in Figure 16 below that an uncompressed video signal is encoded and compressed to encode the input video. *Id.*, ¶¶[0009]; [0059]. Figure 16 shows video communications system 10 includes transmitter side 12 including a video coding layer (VCL) that encodes the input video. *Id.*, ¶[0059].

2. **[9A] “identifying in said encoded video signal an indication that encoded virtual reference data has been incorporated therein, wherein said encoded virtual reference data does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof;”**

Caglar teaches this claim because it discloses a decoder that identifies a header (the claimed “indication”) that indicates the use of a virtual reference frame (the claimed “encoded virtual reference data”) in a macroblock, where the virtual reference frame is not to be displayed. Ex-1003, ¶130.

Caglar discloses the claimed “identification,” because *Caglar* discloses that its “*pictures are encoded in such a way that they comprise picture headers.*” Ex-1005, ¶[0276]. (emphasis added). Specifically, *Caglar* discloses the header includes “a particular value is included to indicate whether the picture uses one or more virtual references frames.” *Id.*

Caglar discloses the claimed “virtual reference data,” because *Caglar* discloses the use of virtual reference frames to encode and decode frames. Ex-1005, ¶¶[0120], [0240]-[0241], [0248]. As discussed above in Section VII.5, in [step 146](#), the encoder encodes a frame INTER format and includes the raw video data and the selected reference frame. *Id.*, FIG. 18a, ¶[0241]. The selected reference frame can be a virtual frame. *Id.*, ¶[0259].

Caglar’s virtual reference frame satisfies the construction of “virtual reference” in the ’960 patent because *Caglar* discloses its “virtual frame is not displayed.” *Id.*, ¶[0127]. Further, *Caglar* discloses “virtual frames are generally not intended to be displayed.” *Id.*, ¶[0201]; *see id.*, ¶¶[0210], [0271]. The construction of “virtual reference” adopted for this IPR is “a group of pixels (e.g., a block) that is used as reference material for encoding portions of the video signal (e.g., a motion-compensated inter-predicted block), but that does not comprise or represent any portion of the actual video sequence to be displayed.” *Caglar*’s virtual frame meets this definition because *Caglar*’s virtual frame is for the encoding and decoding of a complete frame, but the virtual frame is not to be displayed. Ex-1003, ¶133. If the Board determines that “virtual reference” should be construed under its plain and ordinary meaning, *Caglar* discloses it because *Caglar* discloses a “virtual reference frame.” *Id.*

Caglar discloses the claimed “identifying in said encoded video signal an indication that encoded virtual reference data has been incorporated therein,” because *Caglar* discloses a decoder that includes steps 216 and 226 of reading the header information. *Caglar* discloses that “[i]f the current frame is in INTER frame format, the reference frame used in its prediction at the encoder, is identified (step 226).” Ex-1005, ¶[0248]. Information in the picture header may contain information of whether the frame is an INTRA frame or an INTER frame. *Id.*, ¶[0246]. Further, for step 226, “[t]he reference frame may be identified, for example, by data present in the bit-stream transmitted from encoder to decoder.” *Id.*, ¶[0248]. A POSA would have understood that the data present in the bit-stream would include header information that indicates the use of one or more virtual reference frames. Ex-1003, ¶134.

Caglar discloses the claimed generated virtual reference data “does not represent any portion of any individual frame of the original video signal which is to be displayed in said subsequent video display thereof,” because, as discussed above in Section VII.2, *Caglar* discloses that its virtual frames are not to be displayed. Ex-1005, ¶¶[0201], [0210], [0271]. To the extent Patent Owner argues that the claimed generated virtual reference data is not constructed based on information from a complete frame, *Caglar* discloses that the virtual frame may be

constructed on the basis of a previous virtual frame as discussed above in Section VII.2.

To the extent Patent Owner argues that *Caglar*'s decoder receiving a macroblock with a header does not disclose "an indication that encoded virtual reference data has been incorporated," *Duvivier* discloses it. *Duvivier* discloses method 800 that describes a process for forming a macroblock. Ex-1006, ¶[0055]. As part of forming the macroblock, [step 810](#) allocates a portion of the storage structure for "storing data of the slice," where the slice is of a video frame, and, in [step 813](#), the method includes storing "additional useful/meaningful data" including "reference frame index data." And, [step 815](#) includes storing "header data for each macroblock." *Id.*, ¶[0056]. FIG. 8 is shown below.

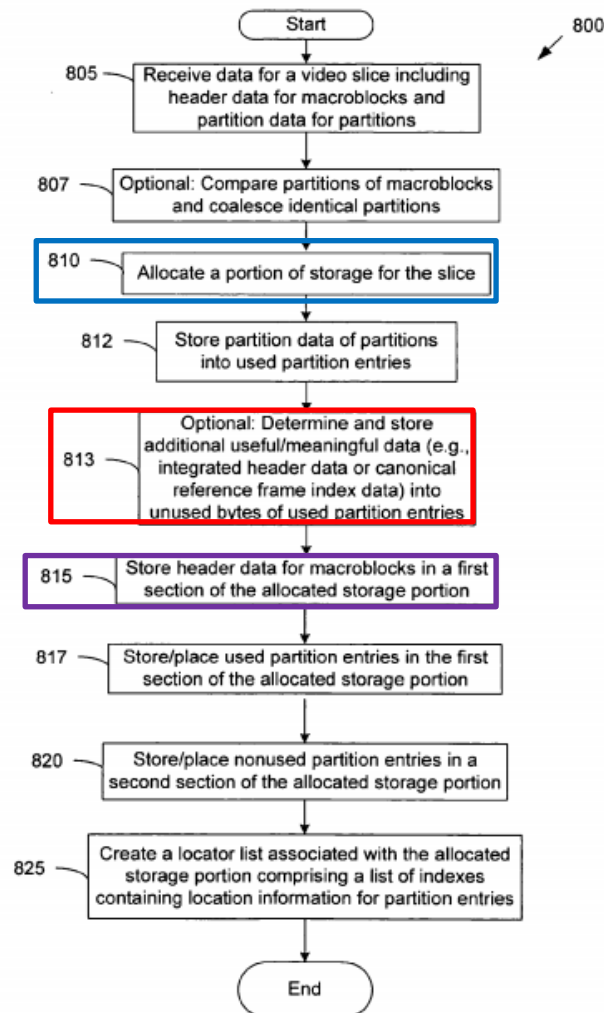


Figure 8

Id., Annotated FIG. 8.

A POSA would have found claim 1 obvious based on *Caglar* and *Duvivier*. Ex-1003, ¶138. And, a POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. *Id.*

In the combination of *Caglar* and *Duvivier*, *Caglar*'s decoder would receive a macroblock including a header (the claimed indication) via the bit-stream. *Id.*, ¶139.

3. [9B] “decoding, using a processor, from said encoded video signal said encoded virtual reference data incorporated therein; and”

Caglar teaches this claim because it discloses a decoder that identifies a header that indicates the use of a virtual reference frame, where the virtual reference frame is not to be displayed. Ex-1003, ¶140.

Caglar discloses the claimed “using a processor,” because *Caglar* discloses the decoding procedure of FIG. 19 is “executed on a general purpose microprocessor or dedicated signal processor (DSP).” Ex-1005, ¶[0262].

As discussed above in Section VII.2, *Caglar* discloses the claimed “virtual reference data,” because *Caglar* discloses the use of virtual reference frames to encode and decode frames. *Id.*, ¶¶[0120], [0240]-[0241], [0248]. As discussed above in Section VII.5, in [step 146](#), the encoder encodes a frame INTER format and includes the raw video data and the selected reference frame, which can be a virtual frame. *Id.*, FIG. 18a, ¶¶[0241], [0259].

Caglar discloses the claimed decoding “from said encoded video signal said encoded virtual reference data incorporated therein,” because *Caglar* discloses decoding a current frame “using the complete received bit-stream and the identified reference frame as a prediction reference (step 234).” *Caglar*, ¶¶[0248]-[0250]. Step 234 is shown in FIG. 19 below.

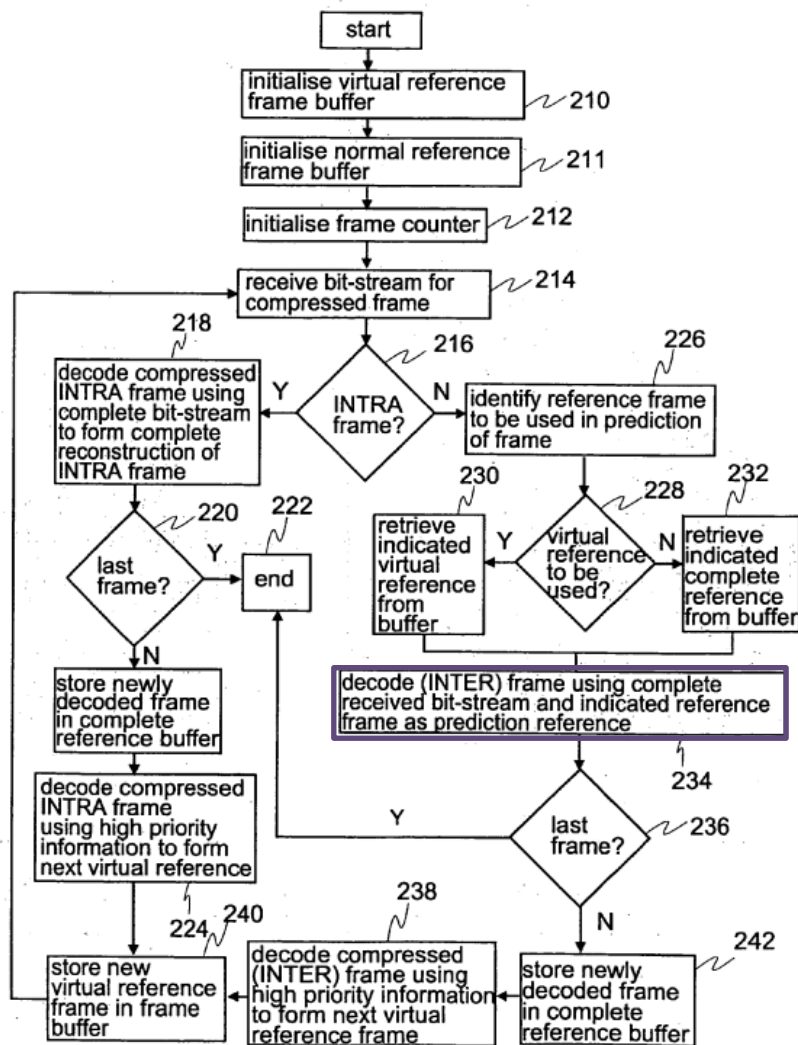


Fig. 19

Ex-1005, Annotated Fig. 19.

To the extent Patent Owner argues that *Caglar*'s decoder receiving and decoding a bit-stream with virtual reference information does not disclose decoding "from said encoded video signal said encoded virtual reference data incorporated therein," *Duvivier* discloses it. As discussed above in Section VII.1, *Duvivier* discloses method 800 that describes a process for forming a macroblock

that includes “reference frame index data.” Ex-1006, ¶[0055], FIG. 8. *Caglar* and *Duvivier* disclose decoding the macroblock including the reference frame data. *Caglar* discloses steps 226 and 228 that use virtual reference frame data from the received bit-stream that is used to decode the current frame in step 234. Ex-1005, ¶¶[0248]-[0250]. In the combination of *Caglar* and *Duvivier*, *Caglar* would receive the same reference frame index data from the bit-stream that it would then use to decode the current frame in step 234. Ex-1003, ¶144.

A POSA would have found claim 9 obvious based on *Caglar* and *Duvivier*. Ex-1003, ¶145. And, a POSA would have been motivated to combine *Caglar* and *Duvivier* as disclosed above in Section 1.2.i. *Id.*

In the combination of *Caglar* and *Duvivier*, *Caglar*’s decoder would receive and decode a macroblock including reference frame index data (the claimed encoded virtual reference data incorporated therein) received via the bit-stream. Ex-1003, ¶146.

4. **[9C] “decoding, using a processor, from said encoded video signal one or more encoded portions of the original video signal which are to be displayed in said subsequent video display thereof, wherein said encoded portions of said original video signal which are to be displayed are based on and specifically reference a portion of said encoded virtual reference data.”**

Caglar teaches this claim because it discloses a decoder, including a microprocessor (the claimed processor), that decodes and reconstructs an encoded

video signal, including a current frame (the claimed one or more encoded portions of the original video signal which are to be displayed), to generate an output video (the claimed subsequent display), where the current frame is based on and identifies the virtual reference frame (the claimed virtual reference data) to encode and decode the current frame. Ex-1003, ¶147.

Caglar discloses the claimed “using a processor,” because *Caglar* discloses the decoding procedure of FIG. 19 is “executed on a general purpose microprocessor or dedicated signal processor (DSP).” Ex-1005, ¶[0262].

Caglar discloses the claimed decoding “from said encoded video signal one or more encoded portions of the original video signal which are to be displayed in said subsequent video display thereof,” because *Caglar* discloses decoding a current frame “*using the complete received bit-stream* and the identified reference frame as a prediction reference (step 234).” *Id.*, ¶¶[0248]-[0250] (emphasis added); Ex-1003, ¶149. **Step 234** is shown in FIG. 19 below.

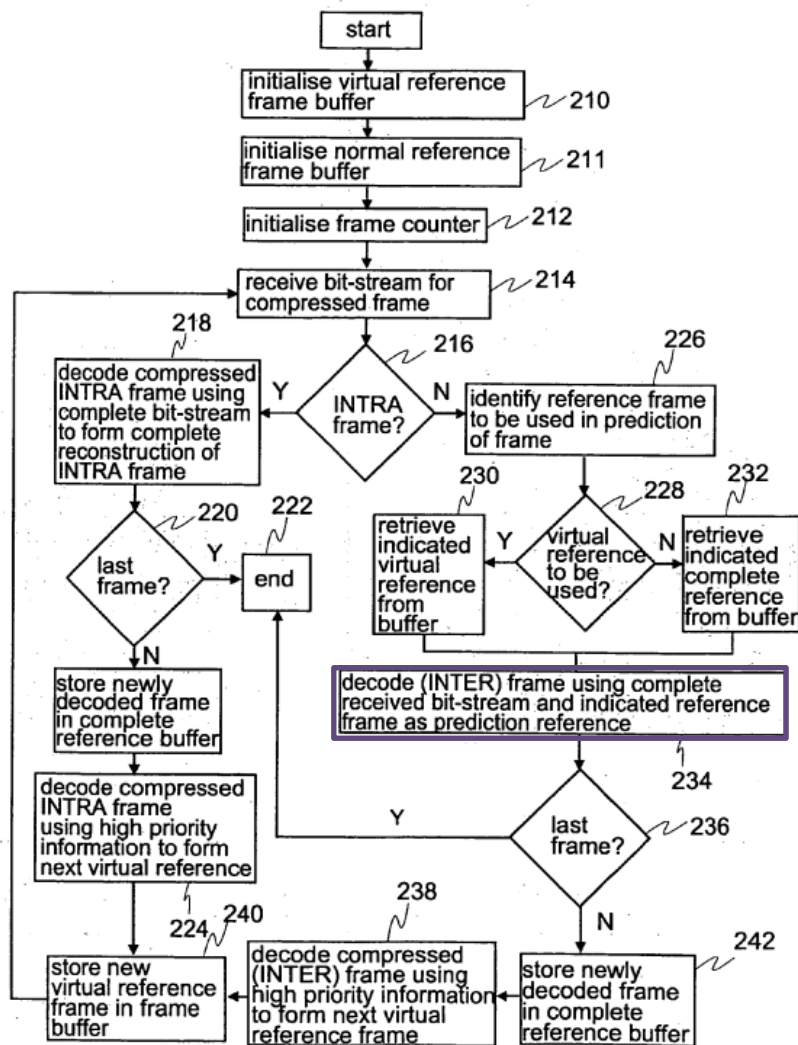


Fig. 19

Caglar, Annotated Fig. 19.

As discussed above in Section VII.6, the frame that is encoded by the encoder and received by the decoder, is a *Caglar* discloses, in [step 146](#), that “[t]he current frame is then encoded in INTER frame format *using the raw video data* and the selected reference frame.” *Id.*, ¶[0241] (emphasis added). Then, in [step 150](#), the bit-stream is formed for transmission to the decoder, *id.*, FIG. 18b,

including that the bit-stream “is arranged in a hierarchical structure with four layers which are, from top to bottom, a picture layer, a picture segment layer, a macroblock (MB) layer, and a block layer.” *Id.*, ¶[0019]. Steps 146, 150, and 152 are shown in FIG. 18 below.

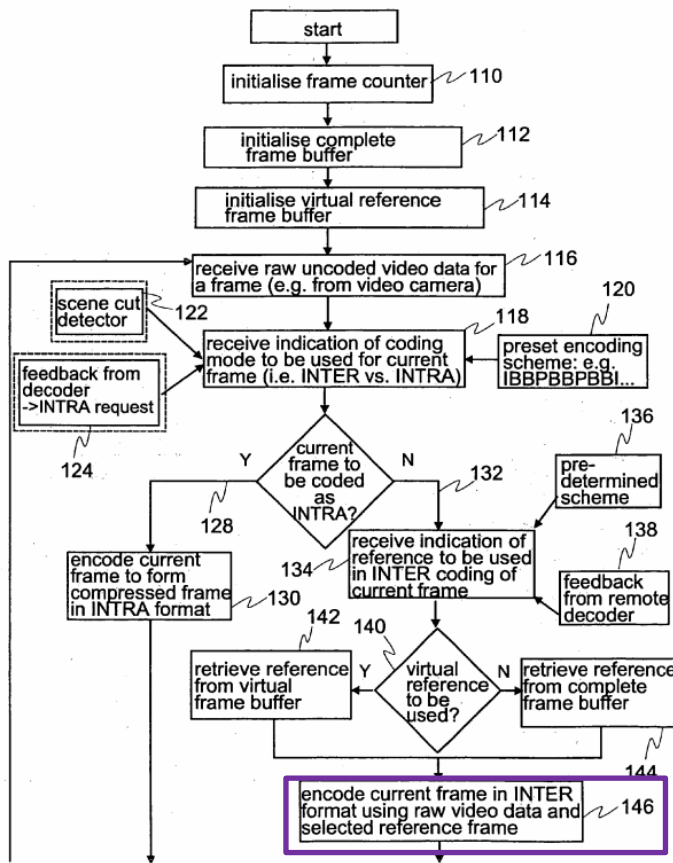


Fig. 18a

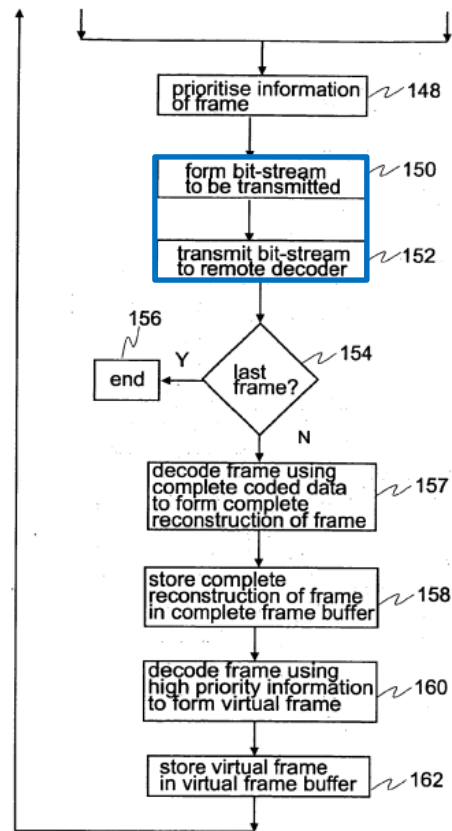


Fig. 18b

(Left) *Caglar*, Annotated Fig. 18a; (Right) *id.*, Annotated Fig. 18b.

The decoded and reconstructed video is then used to generate an output video. Ex-1005, FIG. 16.

Caglar discloses the claimed decoding “wherein said encoded portions of said original video signal which are to be displayed are based on and specifically

reference a portion of said encoded virtual reference data,” because *Caglar* discloses that “[i]f the current frame is in INTER frame format, the reference frame used in its prediction at the encoder, is identified (step 226).” *Id.*, ¶[0248]; Ex-1003, ¶152. Information in the picture header may contain information of whether the frame is an INTRA frame or an INTER frame. Ex-1005, ¶[0246]. Further, for step 226, “[t]he reference frame may be identified, for example, by data present in the bit-stream transmitted from encoder to decoder.” *Id.*, ¶[0248]. A POSA would have understood that the data present in the bit-stream would include header information that indicates the use of one or more virtual reference frames. Ex-1003, ¶152. *Caglar* discloses that “[a]ssuming that the current frame is not the last frame, the bit-stream representing the current frame is then decoded using high priority data in order to form a virtual reference frame (step 238).” Ex-1005, ¶[0251].

G. [Claim 10]

Caglar discloses an encoding method according to FIG. 18 discussed above in Section I.B for claim 2. Claim 10 is substantially similar to claim 2, Ex-1003, ¶155, and thus Petitioner relies on the argument above for claim 2 and the arguments here. Ex-1003, ¶¶153-55. Regarding the claimed “decoding from said encoded video signal said one or more encoded portions of the original video signal which are to be displayed comprises performing block-based motion

compensation on the decoded virtual reference data,” *Caglar* discloses the bit-stream may be different reference virtual pictures “for motion compensation.” Ex-1005, ¶¶[0168], [0286]. Additionally, a POSA would have found it obvious to decode the encoded video signal and use block-based motion compensation on the decoded virtual reference frames. Ex-1003, ¶155.

H. [Claim 11] “The method of claim 9 further comprising the step of storing said decoded virtual reference data in a reference frame buffer.”

Caglar teaches this claim because it discloses storing the decoded virtual reference frame in a virtual reference frame buffer. Ex-1003, ¶156. *Caglar* discloses that “[a]ssuming that the current frame is not the last frame, the bit-stream representing the current frame is then decoded using high priority data in order to form a virtual reference frame (step 238).” Ex-1005, ¶[0251]. Then, “[t]his virtual reference frame is then stored in the virtual reference frame buffer (step 240).” *Id.*

I. [Claim 12]

Caglar teaches this claim because claim 12 is substantially similar to claim 6. Ex-1003, ¶¶157, 158. Thus, Petitioner relies on the arguments above in Sections VIII.C and I.F for claim 6.

J. [Claim 13]

Caglar teaches this claim because claim 13 is substantially similar to claim 7. Ex-1003, ¶¶159, 160. Thus, Petitioner relies on the arguments above in Sections VIII.C and I.F and the argument here. The claimed “wherein the method further comprises the step of relocating the decoded virtual reference data based upon said motion vector” is rendered obvious by the combination of *Caglar* and *Duvivier* that would include *Duvivier*’s step of “when some or all partitions of the same macroblock have the same motion vectors and the same reference frame indexes partitions), the identical partitions are grouped (coalesced) into a single partition for decoding purposes.” Ex-1006, ¶[0098]. A POSA would have understood that *Duvivier* discloses moving a virtual reference frame into a coalesced block based on the motion vector. Ex-1003, ¶159.

K. [Claim 14]

Caglar teaches this claim because claim 14 is substantially similar to claim 8. Ex-1003, ¶¶161, 162. *See also* Sections VIII.C and I.F.

L. Claims 15, 16, 20-22

Caglar anticipates and/or renders obvious claims 15, 16, and 20-22. Ex-1003, ¶163. The limitations of claims 15, 16, and 20-22 are substantially similar to those of claims 1, 2, and 6-8, respectively, except that claims 15, 16, and 20-22 are a “video encoder configured to” perform the same functionality claimed in claims

1, 2, and 6-8, and include the elements of claim [15A] discussed below; thus, Petitioner relies upon the arguments set forth above in Sections VII.A-E for claims 1, 2, and 6-8 and the argument below regarding the claimed “video encoder” and the elements of claim [15A]. Ex-1003, ¶166 (comparing claims); *see Smart Sys. Innovations.*, 873 F.3d at 1368 n.7 (Fed. Cir. 2017), which determined that “[b]ecause the system claim and method claim contain only minor differences in terminology but require performance of the same basic process, they should rise or fall together.”

Caglar discloses the claimed “video encoder” because *Caglar* discloses the methods of encoding such as the steps of FIG. 18, discussed above, that are implemented by “a video encoder.” Ex-1005, ¶¶[[0170], [0179], [0189], [0237].

1. [15A] “a processor and a memory, the memory including machine-executable code which when executed configures the processor to,”

Caglar teaches this claim because *Caglar* discloses a microprocessor (the claimed processor) and that its encoding method may be a computer program stored on a data storage medium (the claimed memory) operated on a computer and including computer executable code. Ex-1003, ¶167.

Caglar discloses the claimed “processor,” because *Caglar* discloses the encoding procedure of FIG. 18 is “executed on a general purpose microprocessor or dedicated signal processor (DSP).” Ex-1005, ¶[0262].

Caglar discloses the claimed “memory including machine-executable code” because *Caglar* discloses machine-executable code used on a computer. *Id.*, ¶[0189]. Specifically, *Caglar* discloses “a computer program for operating a computer as a video encoder for encoding a video signal to produce a bit-stream” and including “computer executable code.” *Id.*, ¶¶[0189]-[0197]. These computer programs are stored on “a data storage medium” *Id.*, ¶[0197]. A POSA would have understood that *Caglar*’s data storage medium is a type of memory. Ex-1003, ¶169.

M. Claims 23-28

Caglar renders obvious claim 23-28. Ex-1003, ¶170. The limitations of claims 23-28 are substantially similar to those of claims 9-15, except that claims 23-28 are a “a video decoder configured to” perform the same functionality claimed in claims 9-15; thus, Petitioner relies upon the arguments set forth above in Sections VII.F-L for claim 9-15 and the argument below regarding the claimed “video decoder” and certain limitations of claim [23p]. Ex-1003, ¶173 (comparing claims); *see Smart Sys. Innovations.*, 873 F.3d at 1368 n.7.

Caglar discloses the claimed “video decoder” because *Caglar* discloses the methods of encoding such as the steps of FIG. 19, discussed above, that are implemented by “a video decoder.” *Caglar*, ¶¶[0160], [0170], [0184], [0237].

1. [23p]

Caglar teaches this claim because *Caglar* discloses a microprocessor (the claimed processor) and that its decoding method may be a computer program stored on a data storage medium (the claimed memory) operated on a computer and including computer executable code. Ex-1003, ¶¶174-76. Petitioner relies on the arguments in Sections VII.1 and I.M for the remaining elements not addressed here. *Caglar* discloses machine-executable code used on a computer and stored on memory to operate its encoder, and a processor that implements computer program code including the decoding method in FIG. 19. Ex-1005, ¶¶[0193]-[0197], [0262]; Ex-1003, ¶¶174-76.

VIII. GROUND 2: CLAIMS 3-5 AND 17-19 ARE UNPATENTABLE OVER *CAGLAR* ALONE OR IN COMBINATION WITH *DUVIVIER* AND *YOUN*

A. Claim 3

- 1. [3A] “The method of claim 2 wherein the step of generating the virtual reference data comprises: identifying a set of video blocks comprising a video block from each of a plurality of video frames represented by said original video signal; and”**

Caglar teaches this claim because it discloses virtual frames can be constructed based on previous virtual frames including using different high priority information of a complete frame. Ex-1003, ¶177.

Caglar discloses the claimed “plurality of video frames represented by said original video signal” because *Caglar* describes an input video that is a sequence of frames. Ex-1005, Abstract, ¶¶[0103], [0111]; Ex-1003, ¶178. *Caglar* discloses, as discussed above in Section VII.1, an input video comprising a sequence of frames.

Caglar discloses an encoding procedure, shown in FIG. 18. *Caglar* discloses that “[t]he procedural steps presented in FIGS. 18 and 19 may be implemented in a video transmission system according to FIG. 16.” Ex-1005, ¶[0237]. *Caglar* discloses that procedure 18 is used to encode raw uncoded video data. *Id.*, FIG. 18a.

Caglar discloses the claimed “identifying a set of video blocks comprising a video block from each of a plurality of video frames” because *Caglar* discloses “a video encoder implemented according to the present invention can be programmed to encode INTER frames P1, P2 and P3 using motion compensated prediction in a prediction chain starting from INTRA frame I0.” *Id.*, ¶[0202]. “Virtual INTRA frame I0' is constructed using the higher priority information representing I0 and similarly, virtual INTER frames P1, P2' and P3' are constructed using the higher priority information of complete INTER frames P1, P2 and P3 respectively and are formed in a motion compensated prediction chain starting from virtual INTRA frame I0” *Id.*

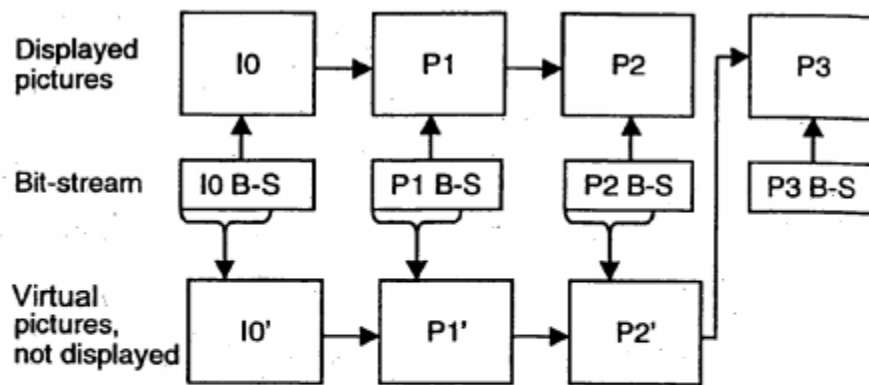


Fig. 21

Id., FIG. 21.

Caglar's disclosure of identifying and selecting virtual frames to generate a virtual frame in the above examples also corresponds to identifying and selecting blocks. Ex-1003, ¶181. *Caglar* discloses that "[t]he selection of the reference frame can be made separately for each frame, picture segment, slice, macroblock, block or whatsoever sub-picture element." Ex-1005, ¶[0167]. *Caglar* discloses that "[r]eference to 'frames' in the context of the invention is intended also to include parts of frames, for example slices, blocks, and [macroblocks] within a frame." *Id.*, ¶[0198]. Accordingly, blocks are parts of frames. *Id.* Accordingly, a POSA would have understood that the method disclosed in FIG. 21 would apply to blocks of frames. Ex-1003, ¶181.

2. [3B] “generating the virtual reference data so as to minimize differences between said identified video blocks and the generated virtual reference data.”

Caglar teaches this claim because it using virtual frames to protect “against errors for transmission.” Ex-1003, ¶182 (citing *Caglar*, ¶[0273]). *Caglar* discloses “the alternative reference frame, that is virtual frame P3', bears a much greater similarity to the reference frame that would otherwise have been used in the prediction of frame P4 (namely, frame P3), than an alternative reference frame (for example P2) that would have been used according to a conventional reference picture selection scheme.” Ex-1005, ¶[0203].

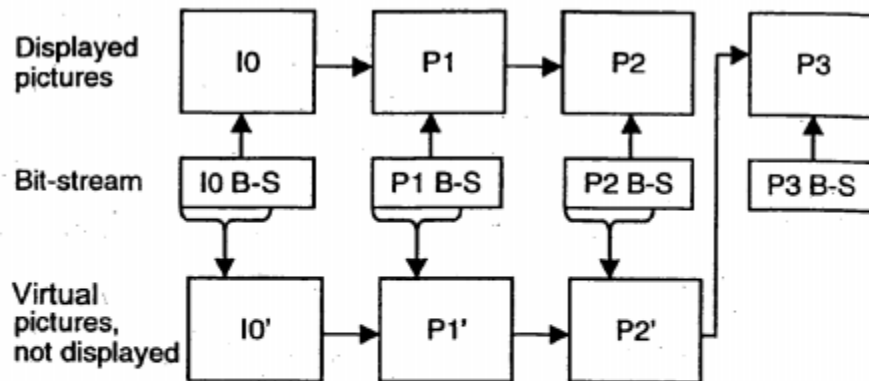


Fig. 21

Id., FIG. 21.

Caglar further discloses that “[t]he use of virtual frames provides a new way of enhancing the error resilience of an encoded bit-stream.” Ex-1005, ¶[0204].

Additionally, a prediction scheme for a frame may be based on previous virtual

frames to “ensure error-free reconstruction.” *Id.*, ¶[0205]. If some frames experience “visual distortion,” the next frame in the sequence may be based on a subset of the previous virtual frames that did not experience the distortion. *Id.*, ¶[0206]. A POSA would have understood that virtual frames would be created to reduce error and distortion would minimize differences between the between the current frame and the virtual frames. Ex-1003, ¶184. A POSA would further understand that the virtual frames are created to bear a great “similarity” to the identified frames. *Id.*

To the extent Patent Owner argues that reducing error and distortion does not disclose the claimed minimizing differences, *Youn* discloses it. *Youn* discloses determining a “transform block that is determined by subtracting a current macroblock (or block) from a predicted macroblock to produce a residual or difference macroblock.” Ex-1009, ¶[0013]. To determine whether to bypass certain computations, either the sum of absolute differences may be found or the sum of absolute transformed differences may be found. *Id.*, ¶¶[0003]-[0004]. The transform block uses “a discrete cosine transform (DCT)” or other transforms to create a block of coefficients. *Id.*, ¶¶[0011]-[0012]. Transform coefficients that are “lower than the lowest decision value are quantified to zero,” *id.*, which is optimal because then “computationally intensive” computations “may be skipped.” *Id.*, ¶[0003]. A POSA would have combined *Caglar* and *Youn* to use *Youn*’s method to

ensure that the predicted macroblock, based on *Caglar*'s virtual reference frame, is similar to the current macroblock and to skip the "computationally intensive" computations. Ex-1003, ¶185.

i. A POSA Would Have Combined *Caglar* and *Youn*

Youn discloses a method of determining whether a transform step and a quantization step may be skipped in order to achieve a more efficient coding and decoding of a video frame. Ex-1009, ¶[0002]. A POSA implementing the method of *Caglar* for encoding a video frame would be motivated to achieve the more efficient coding and decoding of a video frame as disclosed by *Youn*. Ex-1003, ¶185. *Youn*'s method of efficiently determining whether to bypass transform and quantization steps meets *Caglar*'s goal of compression efficiency which "is an important parameter in video transmission systems." Ex-1005, ¶[0008]. A POSA would have recognized that such an implementation would have been a common sense and predictable design choice because *Caglar*'s encoding and decoding methods apply to blocks, Ex-1005, ¶¶[0019], [0198], and *Youn* discloses a method of using the SATD value on blocks to determine whether to bypass computationally intensive transform and quantization steps. Ex-1009, FIG. 2, ¶[0003]; Ex-1003, ¶185. A POSA would have had a reasonable expectation of success because *Youn* and *Caglar* disclose video coding and decoding methods according to H.26x, and *Youn*'s techniques apply to other video coding standards.

Ex-1003, ¶185 (citing Ex-1009, ¶[0002], [0017], [0065]; Ex-1005, ¶¶[0017], [0059]).

B. [Claim 4] “The method of claim 3 wherein the generated virtual reference data comprises block transform coefficient values, and wherein the step of generating the virtual reference data comprises the step of determining a plurality of modal coefficient values based on said set of identified video blocks for use as said virtual reference data.”

Caglar teaches this claim because *Caglar* discloses determining quantized discrete cosine transform coefficients. Ex-1003, ¶183. To the extent Patent Owner argues that reducing error and distortion does not disclose the claimed minimizing differences, *Caglar* in view of *Youn* renders it obvious. Ex-1003, ¶183.

The '960 patent discloses creating “a block of coefficient values--for example, DCT (Discrete Cosine Transform) or similar coefficients, fully familiar to those of ordinary skill in the art.” Ex-1001., 9:66-10:5. The '960 patent refers to “modal coefficient values” only in the claims. The '960 patent does describe that its transform process typically results in a bimodal set of transform coefficients, where blocks are either considered “small error” coefficients, with an absolute value less than or equal to 1, or “large error” coefficients, with coefficients having an error with an absolute value greater than 1. *Id.*, 10:43-50.

Caglar renders obvious the claimed “generated virtual reference data comprises block transform coefficient values.” Ex-1003, ¶185. *Caglar* discloses

that “[b]lock layer data consists of uniformly quantized discrete cosine transform [DCT] coefficients...as explained in detail in ITU-T recommendation H.263.” Ex-1005, ¶[0026]. This is consistent with the ’960 patent’s disclosure that “[t]he use of frequency transform coefficients for coding video signals is fully familiar to those of ordinary skill in the art.” Ex-1001, 9:60-62. A POSA would have found it obvious that any block used in *Caglar*’s encoding method would include quantized DCT coefficients. Ex-1003, ¶188.

Youn disclose the claimed “modal coefficient values” because *Youn* discloses “a method for determining if a bypass should be performed” based on whether DCT coefficients may be quantized to “0” or not. Ex-1009, ¶¶[0016], [0022]. *Youn* discloses using a threshold value to determine whether DCT coefficients may be quantized to “0.” *Id.*, ¶[0016]. Accordingly, a POSA would have understood that *Youn* discloses a bimodal system where DCT coefficients are either below a threshold (difference of current frame and reference frame is small) or above a threshold. *Id.*, ¶¶[0016], [0022], [0027]. Other than using a threshold, *Youn* discloses that the lowest value coefficient may be used to either quantize coefficients as “0” or not. *Id.*, ¶[0030]. Thus, a POSA would have understood *Youn* discloses “modal coefficient values.” Ex-1003, ¶189.

Yuon discloses the claimed “the step of generating the virtual reference data comprises the step of determining a plurality of modal coefficient values based on

said set of identified video blocks for use as said virtual reference data.” Ex-1003, ¶190. As disclosed above, *Youn* discloses a system that finds “a transform of a block of coefficients.” Ex-1009, ¶[0011]. *Youn* discloses that the transform occurs “such that previous frames can be reconstructed and a motion estimation can be determined.” *Id.*, ¶[0015]. Thus, the coefficients are created for use later for motion estimation (i.e. the claimed for use as said virtual reference data). Ex-1003, ¶190. *Youn* discloses “the motion estimation may use either a sum of absolute difference (SAD) or an [sum of absolute transform differences] (SATD) value...[which] provide the prediction in the video coding.” *Id.*, ¶[0021]. Accordingly, a POSA would have understood that the transform coefficient values found using *Youn* are used for motion estimation prediction. Ex-1003, ¶190. A POSA would have created these coefficient values in a combination of *Caglar* and *Youn* to use *Youn*’s method to ensure that the predicted macroblock, based on *Caglar*’s virtual reference frame, is similar to the current macroblock and to skip the “computationally intensive” computations. *Id.*

A POSA would have been motivated to combine *Caglar* and *Youn* as disclosed above in Section 1.2.i. Ex-1003, ¶191.

- C. [Claim 5] “The method of claim 4 wherein the step of generating the virtual reference data further comprises the step of modifying the plurality of modal coefficient values based on a corresponding**

plurality of counts of coefficient values whose absolute difference from said corresponding modal coefficient values exceeds one.”

The combination of *Caglar* and *Youn* renders obvious this claim. Ex-1003, ¶192. *Youn* teaches this claim because *Youn* discloses that when the bypass is not performed, the coefficients, measured in absolute difference, greater than a threshold are transformed. *Id.*

Youn renders obvious the claimed “generating the virtual reference data further comprises the step of modifying the plurality of modal coefficient values based on a corresponding plurality of counts of coefficient values” because *Youn* discloses carrying out “the computations performed by transform module 104 and quantization module 106” and including inverse quantization and transforms based on whether the transformed block coefficients may be quantized to zero. Ex-1009, ¶[0027]. This process corresponds to the claimed “modifying the plurality of modal coefficient values” because the block coefficients are transformed and quantized. Ex-1003, ¶193. If coefficient values can be quantized to “0” (they fall below a threshold), then no steps and modification is necessary. Ex-1009, ¶[0026]; FIG. 2. If not, steps 104 and 106 transform and quantize the coefficient values. Ex-1009, ¶[0027]; FIG. 2.

Youn renders obvious the claimed “modal coefficient values based on a corresponding plurality of counts of coefficient values whose absolute difference

from said corresponding modal coefficient values exceeds one” because *Youn* discloses “a method for determining if a bypass should be performed” based on whether DCT coefficients may be quantized to “0” or not based on a threshold or lowest coefficient number. *Youn* discloses using a measure of absolute difference via the use of sum of absolute differences (SAD) or a sum of absolute transformed differences (SATD). *Id.*, ¶¶[0003]-[0004]. A POSA would have understood that a threshold could be set to one, and so *Youn*’s coefficient values whose absolute difference exceeded one would be modified. Ex-1003, ¶194. A POSA would have created these coefficient values in a combination of *Caglar* and *Youn* to use *Youn*’s method to determine whether to skip the “computationally intensive” computations. Ex-1003, ¶194.

A POSA would have been motivated to combine *Caglar* and *Youn* as disclosed above in Section 1.2.i. Ex-1003, ¶195.

D. Claims 17-19

Caglar alone and/or in combination with *Youn* renders obvious claims 17, 18. Ex-1003, ¶196. *Caglar* in combination with *Youn* renders obvious claim 19. *Id.* The limitations of claims 17-19 are substantially similar to those of claims 3-5, except that claims 17-19 are a “method of” performing the same functionality claimed in claims 3-5; thus, Petitioner relies upon the arguments set forth above in

Sections VIII.A-C for claims 3-5. Ex-1003, ¶198 (comparing claims); *see Smart Sys. Innovations.*, 873 F.3d at 1368 n.7.

IX. NON-INSTITUTION UNDER 35 U.S.C. §§ 314 OR 325 WOULD BE IMPROPER

Non-institution under 35 U.S.C. §§ 314(a) or 325(d) would be improper. The existence of parallel district court proceedings should not prevent institution of this Petition. *Cf. NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8, at 19-20 (PTAB Sept. 12, 2018); *see also* Litigation. No factor favors denial of institution because, at this time, there is no investment beyond the initial discoveries at the district court and this IPR petition. Moreover, the strong merits of this case favor institution.

A. Non-Institution Under 35 U.S.C. §314(a) Is Improper

First, non-institution under 35 U.S.C. §§ 314(a) would be improper. Under the factors articulated in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020 (precedential), non-institution in light of the litigations would be improper because Factors 2-4 and 6 of the *Fintiv* factors favor institution, and Factors 1 and 5 are neutral.

Factor 1 (district court stay) is neutral. While ZTE moved to stay on December 30, 2020, *see* Litigation, Dkt. 47, there remains no indication that the district court will grant or deny the motion to stay. *Int'l Bus. Machines Corp. v.*

Trusted Knight Corp., IPR2020-00323, Paper 15 at 9 (PTAB Jul. 10, 2020). As discussed below, the motion to stay is based on ZTE's pending Motion to Dismiss for Improper venue under § 1400, which unlike venue for convenience under § 1404, is not discretionary. *See* Litigation, Dkt. 45.

Factor 2 (proximity to district court trial) favors institution. The pending district court case is not scheduled for trial until June 20, 2022, and this date is subject to delays. Therefore, the Board will likely issue a final written decision before the pending district case. ZTE has moved to dismiss based on improper venue, and further moved to stay until venue is set. These motions are currently pending, making it “unclear that the court in the related district court litigation will adhere to any [future] scheduled jury trial date.” *Sand Revolution II, LLC v. Cont'l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24, at 9 (PTAB June 16, 2020) (informative). Should the district court grant either of the pending improper venue motion or the motion to stay, these cases will be assigned new, later trial dates likely in a new forum. Additionally, it is further noted that Judge Albright is unable to maintain trials based on their originally scheduled dates and is delaying the trials. As one example, the *VLSI Tech. LLC v. Intel Corp.*, No. 1:19-cv-00254 (W.D. Tex.) trial this month was delayed four months from its original date in October 2020.

Factor 3 (investment in district court case) favors institution. The parties' and the court's investment in this case has been minimal. *Fintiv*, Paper 11, at 11. Although preliminary infringement and invalidity contentions have been served, claim construction has only just begun, and the claim construction hearing is not scheduled to occur for another two months in May 2021. In addition, the parties have not conducted any substantive fact discovery, as fact discovery does not open until after the claim construction hearing. Finally, the district court has not addressed the substance of the '960 Patent—Patent Owner did not move for a preliminary injunction, and Defendants did not move to dismiss Patent Owner's action based on the substance of the '960 Patent, such as a motion to dismiss based on § 101. Where, as here, "the district court has not issued orders related to the patent at issue in the petition, this fact weighs against exercising discretion to deny institution." *Fintiv*, Paper 11, at 10.

Factor 4 (overlapping issues) favors institution. WSOU is a prolific filer of patent infringement lawsuits. Based on WSOU's litigation activity, it is likely that WSOU will bring more suits against other parties based on the '960 patent. Resolving the invalidity questions raised herein would mitigate any concern of duplicative efforts in the future. Additionally, ZTE will stipulate that, if this IPR is instituted, it will not pursue the specific grounds identified in this Petition

(Sections VII-VIII) before the district court. This stipulation mitigates any concern of duplicative efforts. *Sand Revolution*, Paper 24, at 11-12.

Factor 5 (whether petitioner is also the defendant in district court) is neutral.

Factor 6 (other circumstances) favors institution. As explained above, the challenged claims are unpatentable over *Caglar*, *Duvivier*, and *Youn*—none of which were considered during prosecution. And, although a non-related party recently filed a petition challenging claims 9-11 and 23-25 of the '960 patent—with only six overlapping challenged claims here—it did not rely on any reference or combination of references cited herein. *See Unified Patents, LLC v. WSOU Investments LLC*, IPR2021-00378. A determination of the '960 validity by the Board here would still save resources in the associated district court, and any additional cases WSOU may bring. There is a significant public interest against “leaving bad patents enforceable,” *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

B. Non-Institution Under 35 U.S.C. §325 Is Improper

Second, Non-institution under § 325 would also be improper based on a weighing of the factors set forth in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017). The asserted combinations are materially different and not cumulative of the prior art involved during the examination of the challenged claims. During prosecution, the following

reference was applied by the examiner: *Su* (Ex-1002, Ex-1013). *Su* describes methods and apparatus using virtual reference pictures, where the “virtual reference pictures (VRPs) are created from already decoded pictures.” *Su*, Abstract, 6:32-33.

The primary references in the asserted combinations, *Caglar*, *Duvivier*, and *Youn* were never listed by the Patent Owner nor cited by the examiner. They were never discussed or applied by the examiner to reject any claims. They are materially different from and not cumulative of the earlier references at least because they describe projection imaging devices that include movement sensors—elements that WSOU argued were missing from *Su*. There is thus little to no overlap between the current and prior arguments. *Becton*, Paper 8, 23. But *Su* teach these added limitations, making denial under § 325(d) improper. Sections VII-VIII.

Furthermore, as addressed above for the *Fintiv* Factor 6, a non-related party filed a petition challenging the '960 patent. See *Unified Patents, LLC v. WSOU Investments LLC*, IPR2021-00378. *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (P.T.A.B. Sept. 6, 2017) identified several factors considered by the Board in exercising its discretion to deny institution of *inter partes* review, including “whether the same petitioner previously filed a petition directed to the same claims of the same patent,” and “whether at the time of filing of the second petition the petitioner already received

the patent owner’s preliminary response to the first petition or received the Board’s decision on whether to institute in the first petition.”

First, the petitioners are different parties. ZTE are not the same petitioners as Unified Patents, LLC (“Unified”). ZTE are not similarly situated to Unified. ZTE have no relationship to the earlier-filed proceeding. ZTE have not joined the earlier proceeding, and ZTE are not a co-defendant in litigation with Unified—in fact Unified is not in any litigation pertaining to this patent (*see* Section X.B). Moreover, ZTE was unaware of the earlier-filed petition before it was filed, and ZTE has not engaged in discussions with Unified regarding the respective petitions. *See Unified Patents, LLC v. WSOU Investments LLC*, IPR2021-00378.

Second, an *inter partes* review based on this petition would not be redundant of the earlier petition. For instance, of the 25 claims challenged here only 6 overlap with the Unified petition, and none of the respective Grounds or references overlap. *Unified Patents, LLC v. WSOU Investments LLC*, IPR2021-00378 (petitioning for *inter partes* review based on combinations involving “*Cheung*,” “*Bankoski*,” and “*Hannuksela*”). Those references disclose systems and methods that function differently from ZTEs’ prior art. As an example, while *Bankoski* describes a method for increasing video compression efficiency by minimizing residual values (IPR2021-00378, p. 17) *Caglar* describes methods for “encoding a video signal” (Ex-1005, ¶¶[0103], [0111]), *Duvivier* describes methods for storing

data for a slice of a video frame where each frame is comprised of multiple macroblocks (*Duvivier*, Abstract, ¶[0004]), and *Youn* discloses efficiencies to be had when comparing a macroblock from an input frame to a predicted macroblock (*Youn*, ¶[0011]).

Further, in neither proceeding has the Board provided any substantive guidance or made an institution decision, nor has Patent Owner submitted a Preliminary Patent Owner Response. ZTE have had no opportunity to learn the Board's or Patent Owner's views in the earlier proceeding.

X. MANDATORY NOTICES

A. Real Parties-in-Interest

The real parties-in-interest are ZTE Corporation, ZTE (USA), Inc., and ZTE (TX), Inc.

B. Related Matters

Patent Owner has asserted the '960 patent in litigation against Petitioners in the Litigation, filed on June 3, 2020. *See also WSOU Investments, LLC v. ZTE Corporation et al.*, 6:20-cv-00228 (WSOU initially asserted the '960 patent against Petitioners on March 26, 2020 and dismissed the case on June 3, 2020).

C. Lead and Back-Up Counsel, and Service Information

Petitioners provide the following counsel and service information. Pursuant to 37 C.F.R. § 42.10(b), Powers of Attorney accompany this Petition. Petitioners

consent to e-mail service at the e-mail addresses identified in the table below, as well as at ZTE-WSOU-IPRs@finnegan.com.

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U.S. Patent 8,179,960

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XI. GROUNDS FOR STANDING

Petitioner certifies the '960 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified in this Petition.

XII. CONCLUSION

Petitioner has established a reasonable likelihood of prevailing with respect to each of the challenged claims 1-25 of the '960 patent. Petitioner therefore requests the Board institute *inter partes* review and cancel each of these claims as unpatentable.

The Office may charge any required fees for this proceeding to Deposit Account No. 06-0916.

Date: March 26, 2021

Respectfully Submitted,

/Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW contains 13,971 words, excluding the parts of this Petition that are exempted under 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

/Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Petition for *Inter Partes* Review, the associated Power of Attorney, and Exhibits 1001 through 1019 are being served on March 26, 2021, by Priority Mail Express or by means at least as fast as Priority Mail Express at the following address of record for the subject patent.

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Daniel E. Doku
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